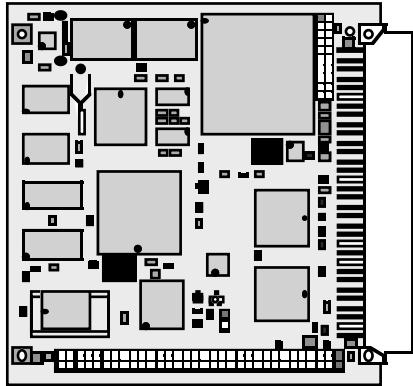
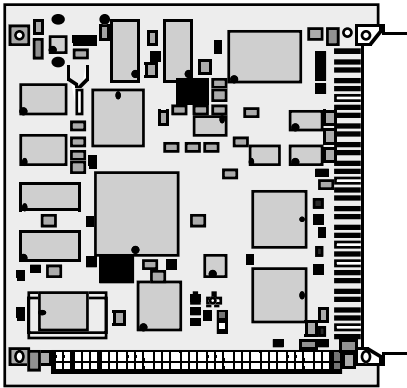


The megatel

PC/+Vs & PC/+Vsc

Technical Manual

megatel computer corporation
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Order Number: MA990627-1.10e

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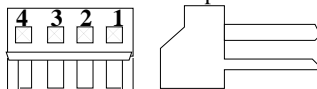
** WARNING **

MAKE SURE:

**The CORRECT VOLTAGE IS APPLIED to the
*PC/+Vs and PC/+Vsc***

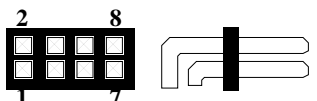
- The voltages required to operate the **PC/+Vs & PC/+Vsc** are +5V and GND.
- Using a QTB/II*, QTB/104* or QTB/104AT* +5V & GND are connected to the **PC/+Vs & PC/+Vsc** via the 96-pin Peripheral Connector and/or the 64-pin ISA Bus Connector.
- One power connector found on the QTB/II, QTB/104 and QTB/104AT is that of a 4-pin male 3.5" floppy-disk styled power connector (QTB/II uses a straight up type connector, whereas the QTB/104 and QTB/104AT use the right angle versions).
Molex Part #53133 for the right angle version, with the mating or "housing" connector Part #5507.
- The total current drawn from the 3.5" floppy-disk styled power connector can exceed 100mA (3A max).
- The QTB/104 and the QTB/104AT have an additional 8-pin (2x4) right angle male header power connector for PC/104 power connection compatibility.

Male Right Angle
3.5" Floppy-styled
Power Connector



1	+5V	3	GND
2	GND	4	+12V

Male Right Angle
PC/104 compatible
Power Connector

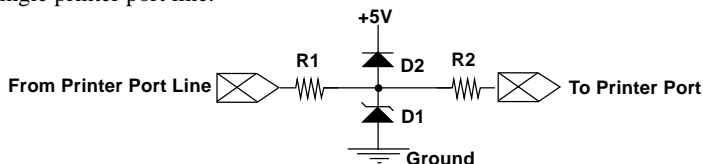


1	GND	5	-5V
2	+5V	6	-12V
3	KEY	7	GND
4	+12V	8	+5V

The *PC/+Vs & PC/+Vsc* is the

FIRST ITEM TURNED ON & the LAST ITEM TURNED OFF

- **NEVER** turn off the *PC/+Vs & PC/+Vsc* when there are other peripherals connected and powered on, such as a printer.
- This is especially important, as the bus and the printer ports are **NOT** buffered†. The unbuffered bus and printer port was done to reduce the power requirement of the board.
- Below is an example of a buffering/filtering circuit which can be used for a single printer port line.



D1: 1N4148 Signal Diode

D2: +5V TransZorb (Transient Voltage Suppressor)

R1 & R2: 27Ω Resistors

***Note:** For more detailed information on the QTB/II, QTB/104 and QTB/104AT, please see your "QTB Manual".

†Note: The ISA Bus Clock is normally buffered

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1.00 Introduction

This is the technical manual for the *PC/+Vs* and the *PC/+Vsc*. Unless otherwise noted, descriptions in this manual apply to both SBC's (Single-Board Computers).

1.01 Introduction to the *PC/+Vs*

The *PC/+Vs* is a surface mounted single-board computer based on the NEC V40H™ microprocessor. It features up to [640k Bytes on-board user DRAM](#), up to [2048k Byte Flash EPROM](#), a [VGA graphics display controller](#) (VGA monochrome LCD Flat panel display video outputs), a [floppy disk controller](#), three asynchronous serial communication ports, one [parallel printer port](#), a [serial keyboard port](#), an [interval timer](#), a [real time clock-calendar with battery back-up](#), a [DMA controller](#), [eight interrupt levels](#), a [speaker output](#), and an [8-bit IBM ISA BUS interface](#).

1.02 *PC/+Vs* General Specifications

CPU & MEMORY:

- V40H CPU
- [20MHz CPU clock frequency](#)
- PC compatible BIOS and Architecture
- 128k-2048k Byte Flash EPROM
- 128k-256k Byte BIOS in ROM
- Up to 1792k Byte User ROM Space
- 640k Byte User DRAM
- 8 Levels of Interrupt (IBM standard)
- 3 DMA Channels
- 3 16-bit Counter Timers

VIDEO CONTROLLER:

- Vadem VGA VG-660 LCD Video Controller
- 256k Bytes of Video DRAM
- Supports Monochrome LCD's
- 16 level grey scale
- Up to 640 x 480 resolution

SCSI DISK CONTROLLER:

- ASPI compatible SCSI Controller
- Standard IBM PC AT Hard Disk BIOS support via SCSI port
- Complete interface for SCSI compatible hard drives
- Multi-media software supports CD ROMs, audio devices and optical storage

INPUT/OUTPUT:

- On-board 8-bit ISA Bus Expansion (supports up to 4 external slots)
- [2 IBM compatible RS-232 Serial Ports](#)
- [1 V40H Serial Port--used via BIOS Calls](#)
- On-board voltage converter for Serial +/- voltages
- Independent software selectable BAUD rates
- Real-Time Clock with Battery Backup
- 8-bit bi-directional Parallel I/O Port with BIOS support as a Printer Port
- Standard IBM Keyboard Port
- Speaker Output and Reset Input

FLOPPY DISK CONTROLLER:

- CMOS Floppy Disk Controller
- Can Use 360k Byte, 720k Byte, 1.2M Byte or 1.44M Byte Drives
- Boots standard versions of PC, MS DOS, or DR DOS
- Supports up to two drives

MISCELLANEOUS:

- Only 100mmx100mm (4" x 4")
- Requires only +5V operation
- Power consumption less than 2 Watts typical (with all options installed)
- Surface Mounted
- Operating Temperature 0°C to +70°C
- Storage Temperature -20° to +85°C

1.10 Introduction to the PC/+Vsc

The PC/+Vsc is a surface mounted single-board computer based on the NEC V40H™ microprocessor. It features up to [640k Bytes on-board user DRAM](#), up to [2048k Byte Flash EPROM](#), a [VGA graphics display controller](#) (VGA monochrome/Color, CRT /LCD Flat panel display video outputs), a [floppy disk controller](#), three asynchronous serial communication ports, one [parallel printer port](#), a [serial keyboard port](#), an [interval timer](#), a [real time clock-calendar with battery back-up](#), a [DMA controller](#), [eight interrupt levels](#), a [speaker output](#), and an [8-bit IBM ISA BUS interface](#).

1.11 PC/+Vsc General Specifications

CPU & MEMORY:

- V40H CPU
- [20MHz CPU clock frequency](#)
- PC compatible BIOS and Architecture
- 128k-2048k Byte Flash EPROM
- 128k-256k Byte BIOS in ROM
- Up to 1792k Byte User ROM Space
- 640k Byte User DRAM
- 8 Levels of Interrupt (IBM standard)
- 3 DMA Channels
- 3 16-bit Counter Timers

VIDEO CONTROLLER:

- Chips & Technology® 65530 CRT/LCD Video Controller
- 256KBytes or 1MByte of Video DRAM
- Supports Color Flat Panels (TFT & STN)
- Supports Analog VGA/SVGA Monitors & LCD, EL & Gas Plasma displays
- Enhanced backward compatibility with EGA™, CGA™, Hercules™, & MDA™ standards
- VGA Register Set Compatible

SCSI DISK CONTROLLER:

- ASPI compatible SCSI Controller
- Standard IBM PC AT Hard Disk BIOS support via SCSI port
- Complete interface for SCSI compatible hard drives
- Multi-media software supports CD ROMs, audio devices and optical storage

INPUT/OUTPUT:

- On-board 8-bit ISA Bus Expansion (supports up to 4 external slots)
- [2 IBM compatible RS-232 Serial Ports](#)
- [1 V40H Serial Port--used via BIOS Calls](#)
- On-board voltage converter for Serial +/- voltages
- Independent software selectable BAUD rates
- Real-Time Clock with Battery Backup
- 8-bit bi-directional Parallel I/O Port with BIOS support as a Printer Port
- Standard IBM Keyboard Port
- Speaker Output and Reset Input

FLOPPY DISK CONTROLLER:

- CMOS Floppy Disk Controller
- Can Use 360k Byte, 720k Byte, 1.2M Byte or 1.44M Byte Drives
- Will boot standard versions of PC, MS DOS, or DR DOS
- Will support up to two drives

MISCELLANEOUS:

- Only 100mmx100mm (4" x4")
- Requires only +5V operation
- Power consumption less than 2 Watts typical (with all options installed)
- Surface Mounted
- Operating Temperature 0°C to +70°C
- Storage Temperature -20° to +85°C

1.20 General System Notes

Power Supply

The *PC/+Vs* & *PC/+Vsc* use +5V \pm 5%.

The voltage Rise Time should be from +2V to +5V within 10ms.

Reset

The /Reset line found at J1, pin 31A (96-pin peripheral I/O connector) should be driven by an open-collector or mechanical switch.

Bus Channel 3

On the ISA Bus, Bus Channel 3 utilizes the 8237A /DACK0 and DREQ0 (instead of /DACK3 and DREQ3). The DMA Page Register (Write-only register) is addressed at 82h. Refresh is handled by the V40H DRAM refresh signal.

1.30 Processor Speed & Wait States

The *PC/+Vs* & *PC/+Vsc* use a 20MHz V40H processor with a CPU clock frequency of 19.091MHz.

No wait states are added to on-board memory operations.

Three wait states have been added to I/O operations and to Memory cycles, for a total of 350 nanoseconds per cycle.

All DMA operations, including memory refreshing, include two wait states. The addition of wait states is possible for the addition of memory-mapped cards using the IBM PC Bus, if required.

A clock cycle on the *PC/+Vs* or *PC/+Vsc* is approximately 70 nanoseconds. A typical I/O instruction has 2 clock cycles or about 140 nanoseconds. This should be good enough for most I/O cards. **megatel** has added 3 wait states for I/O. This gives 350 nanoseconds which should be ample for most I/O cards (A 4.77 MHz PC allows about 400 nanoseconds).

1.31 V40H™ Special Registers

The V40H™ is a processor with some special features for different applications. They are as follows in [Table 1.00](#).

Table 1.00 V40H™ Special Functions (*description*)

I/O Register	Name	Description
FFFF	Reserved	Reserved
FFFE	OPCN	On-Chip Peripheral Connection Register. Selects between DMA3 and V40 Serial Port.
FFFD	OPSEL	On-Chip Peripheral Selection. Enables SCU, TCU, ICU, DMAU.
FFFC	OPHA	On-Chip Peripheral High Address. Sets the upper byte of the I/O Address assigned to the SCU, TCU, DMAU.
FFFB	DULA	DMAU Low Address. Sets the lower byte of the I/O address assigned to the DMAU.
FFFA	IULA	ICU Low Address. Sets the lower byte of the I/O address assigned to the ICU.
FFF9	TULA	TCU Lower Address. Sets the lower byte of the I/O address assigned to the TCU.
FFF8	SULA	SCU Lower Address. Sets the lower byte of the I/O address assigned to the SCU.
FFF7	Reserved	Reserved
FFF6	WCY2	Wait Cycles 2. Sets the number of wait cycles for DMA and Refresh Cycles.
FFF5	WCY1	Wait Cycles 1. Sets the number of wait cycles for each of the three memory regions and for I/O Cycles.
FFF4	WMB	Wait Memory Boundary. Defines the boundary addresses of the three memory wait state regions.
FFF3	Reserved	Reserved
FFF2	RFC	Refresh Control. Enables/ Disables refresh by the RFU and sets the refresh interval.
FFF1	Reserved	Reserved
FFF0	TCKS	Timer clock selection. Selects the clock source (internal or external) for the TCU and the divisor by which the frequency of the internal clock is divided.
FFEF	Reserved	Reserved
FFEE	Reserved	Reserved
FFED	Reserved	Reserved

continued on next page

Table 1.00 V40H™ Special Functions (*description-continued*)

I/O Register	Name	Description
FFEC	WSMB	Wait Sub-Memory Block Register. Specifies a size of the upper and lower sub-memory blocks (USMB & LSMB)
FFEB	WIOB	Wait I/O Block Setting Register. Sets a size of the upper (UIOB) and lower (LIOB) I/O blocks in 3 divided I/O areas, where the area between the upper and lower blocks is the middle block.
FFEA	WCY3	Wait Cycle Number Setting Register 3. Sets UIOW, LIOW, USMW and LSMW wait states.
FFE9	BRC	Baud Rate Counter. Sets the scaling factor for the internal clock (fixed at 1/2 the oscillator frequency).
FFE8 to FFE2	Reserved	Reserved
FFE1	BADR	Bank Address Register. Selects the I/O address of the bank register.
FFE0	BSEL	Bank Address Select. Specifies the Address of the Bank Registers BNKR0 to BNKR3 on Channel0 to Channel3.

1.40 V40H Serial Port and DMA Channel 3

The V40H serial port (COM 4) and DMA channel 3 cannot be used simultaneously because of internally shared I/O lines. **megatel** opted for the additional I/O serial port with memory refresh being handled by the V40H DRAM refresh signal (usually, memory refresh is handled by /DACK0 of the 8237A). [See Table 2.00](#)

Note: On the ISA Bus Channel3 utilizes the 8237A /DACK0 and DREQ0 (instead of using /DACK3 and DREQ3). The DMA Page Register (Write-only register) is addressed at 82h.

Table 2.00 DMA Channel and Page Registers

Function	8237A Channel Name	ISA Bus /DACK Used	ISA Bus DREQ Used	DMA Page Register Address (Hex)
V40H-Com4	3	N/A	N/A	N/A
Floppy	2	/DACK2	DREQ2	81
Unused	1	/DACK1	DREQ1	83
SCSI & 8237A Bus Channel 3	0	/DACK3	DREQ3	82

1.50 Main Memory

Main memory consists of two (2) pieces of 1Megx4 CMOS DRAM's, in a TSOP package.

640kB of memory is addressable from [00000h to 9FFFFh](#)

The BIOS automatically checks the memory at Power-On to determine the amount of RAM available. No straps or jumpers are needed to specify the size of the Main Memory. This is all handled internally by **megatel's** Custom ASIC.

1.51 EPROM Memory

The standard EPROM installed is a 1Mbit (128KByte) E28F010 Flash EPROM which contains the BIOS (including the VGA BIOS and SCSI Option ROM) for the system.

Utilizing the E28F010 Flash EPROM, allows 128KBytes of address space to be used by the PC Bus ([C0000h to DFFFFh](#)).

Utilizing a 2Mbit (256KByte) E28F020 Flash EPROM allows 128KBytes of address space to be used as EPROM Option Rom Space.

An alternative to installing the 128KByte or the 256KByte EPROM is to install a Flash Disk. The Flash Disk is available as an 8Mbit (1MByte) 28F008 or 16Mbit (2MByte) 29F016 Flash Disk. Under these circumstances, the 128KBytes of address space (C0000h to DFFFFh) is enabled to the Flash Disk.

The E28F010 and E28F020 Flash EPROMs are in a PLCC package. The 28F008 and the 29F016 Flash EPROM are in a TSOP package.

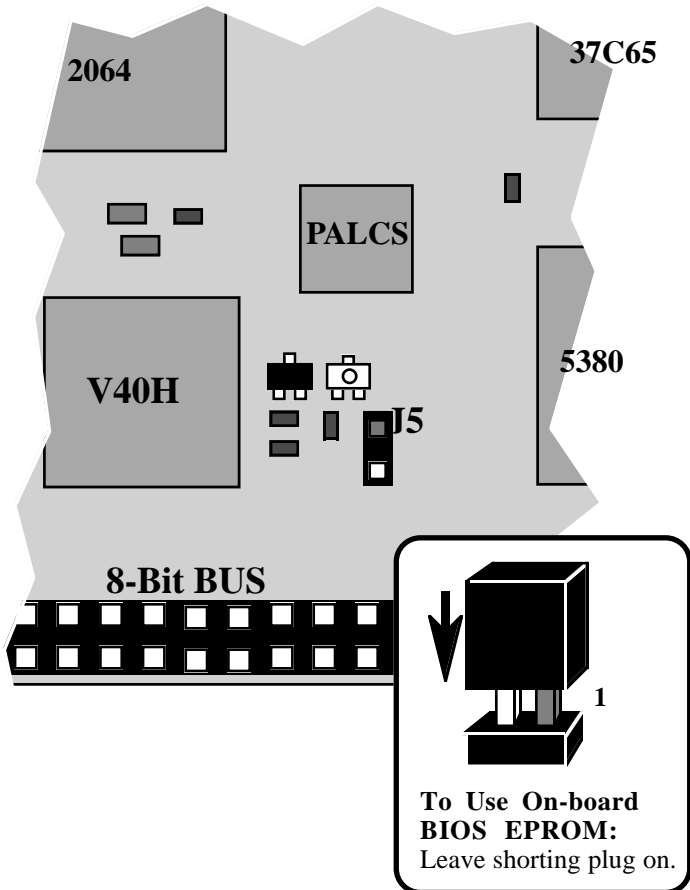
Also see "[4.00 System Memory Map: With On-Board Video](#)" chapter.

1.52 Disabling the On-Board Flash EPROM

The on-board Flash EPROM is usually soldered onto the board thus, a 2-pin shorting jumper has been installed to allow an external EPROM, *which contains our BIOS*, to be used via the bus. The Flash EPROM disable jumper is located between the V40H CPU, 16V8 GAL (PALCS), 5380, and the PC BUS header. To disable the on-board Flash EPROM, remove the shorting plug. This disconnects the Chip select line of the Flash EPROM from A19.

This is used strictly by megatel and must be installed in order for the PC/+Vs or PC/+Vsc to function properly.

DO NOT REMOVE.



1.60 Interrupts

The V40H Programmable Interrupt Controller provides eight interrupt levels and is found at [I/O address 020h to 021h](#). The V40H Non-Maskable Interrupt (NMI) is also used as an interrupt function. The eight Interrupt Request (IRQ) inputs and an NMI are assigned as shown in [Table 3.00](#).

There are two possible sources for the NMI interrupt. One of these is the V40H DMA NMI and the other is a PC Bus Error, which sets the PC Bus Check flag. The NMI service routine should check the PC Bus Check Flag (bit 6 or 7 in [Port 062h](#)) to determine whether the source of an NMI interrupt is a V40H DMA NMI or an I/O Channel Error.

The NMI interrupt can be masked off by the NMI Mask. When the NMI Mask is reset, the NMI input to the V40H is disabled and an I/O Channel Error at this point, would not be able to generate an NMI to the CPU. When the NMI Mask is set, an I/O Channel Error would be able to generate an NMI to the CPU. The NMI Mask is controlled by bit 7 of the NMI Mask register ([I/O address 0A0h](#)). Writing 80h to the NMI Mask register at address 0A0h enables the NMI, while writing 00h to the same register disables the NMI.

Table 3.00 Interrupt Assignments

IRQ#	Function
0	Timer 0 output
1	Keyboard interrupt
2	PC Bus & V40H Serial Channel interrupt DTR (COM4) & Video Controller (VG-660 or 65550)
3	PC Bus & Secondary Asynchronous Serial Channel interrupt (COM 2)
4	PC Bus & Primary Asynchronous Serial Channel interrupt (COM 1)
5	PC Bus & SCSI interface
6	PC Bus & Floppy Disk controller
7	PC Bus & Parallel Printer
NMI	V40H DMA or PC Bus I/O Check

1.70 Interval Timer

Internal to the V40H is the equivalent of one Intel 8253 Programmable Interval Timer and has an [I/O address of 040h to 043h](#). The V40H has three 16-bit counter/timers. Timer 0 & Timer 2 are clocked by a 1.193 MHz clock, resulting in a minimum timing resolution of 838ns. Timer 1 is clocked from the CPU clock, divided by 2 (4.07MHz). The Gate inputs for Timer 0 and Timer 1 are tied high. The Gate input for Timer 2 are controlled by the Timer 2 Gate Bit, which is Bit 0 of [Port 061h](#).

The output from Timer 0 is connected to interrupt input [IRQ0](#) on the Interrupt Controller. This timer is used by the operating system for its internal real-time clock.

The output from Timer 1 is used to generate the Baud rate for serial channel [COM 4](#).

Timer 2 is used to generate signals for the Speaker output. The Timer 2 output is gated with the SPEAKER DATA bit (bit 1 of [Port 061h](#)) to drive the SPKR output. The combination of the Timer 2 Gate control bit and the SPEAKER Data bit allow complex waveforms to be generated on the [Speaker output](#). The state of the TIMER 2 output can be read at [Port 062h](#) bit 5.

The Speaker output, SPKR, is pin A9 of J1. It is intended to drive a piezo-electric audio transducer connected between the SPKR pin and ground.

1.80 Real Time Clock

The Real-time Clock uses a Dallas DS1307 Serial Real Time Clock chip along with a 32.768kHz crystal and a 3.0V Lithium battery. The battery is soldered onto the circuit board over the clock chip.

Clock chip features include:

- 64 x 8 battery backed up CMOS RAM
- Low standby current
- Four Year Calendar
- 24 or 12 Hour Format
- Automatic word address incrementing
- Programmable alarm, timer, and interrupt function

The clock comes set at proper date and time from the factory for North American EST. The software for the clock is included as part of the BIOS with boards containing the Real-Time-Clock option. Standard features of the RTC option include both leap year and year changeover.

The DOS clock is updated automatically by the RTC upon Boot Up. Should you change the time or date in DOS, the *PC/+Vs* & *PC/+Vsc* will conversely update the RTC chip. The *PC/+Vs* & *PC/+Vsc* use standard DOS instructions to change the time and the date. If you are using standard DOS where the time and date are displayed upon boot up, you may change the time and date at this point. While in DOS, the time and date can also be changed by typing TIME, then entering the desired time and typing DATE, then entering the desired date.

The 64 Bytes of battery backed CMOS RAM is also used to store information pertaining to the CMOS RAM SETUP & LCD Driver file values.

The CMOS RAM SETUP includes such information as the time and date; the amount of useable memory available; video mode (monitor type); floppy disk drive type and whether there is one or two drives connected. (*For more information regarding the CMOS RAM SETUP, please read the CMOS RAM Setup section of the "PC/+v & PC/II+ Series Products User's Manual"*).

When using an LCD panel, a driver file must be loaded into the *PC/+Vs* VG-660 Video controller registers or the *PC/+Vsc* 65530 Video controller registers. The LCD driver file values are stored in the CMOS RAM of the Real-Time Clock and loaded into the proper VG-660 or 65530 registers upon boot up.

The real time clock Control & Data Port is at [I/O address is 070h-071h](#). The real time clock memory map, is found in the "[1.83 Real Time Clock Memory Map](#)" chapter.

The 3.0V Lithium battery is rated for 190mAh (typical) in an operation temperature range of -20°C to +70°C. The storage temperature range is -40°C to +60°C and the Self discharge is less than 1% per year at 25°C. It is intended for use with the Real-Time Clock only.

continued on next page

1.81 Real Time Clock Interrupt 1AH

Some of the AT compatible clock functions are implemented. The AT compatible clock functions implemented are 0 to 9.

AT compatible clock functions 2 & 3 are supported, but the Daylight Savings Time Option is not implemented. AT compatible clock function 9 is also supported where the Alarm Status becomes: 0=Alarm not enabled, 1=Alarm enabled-Time not reached, 3=Alarm enabled-Time reached

CLKGET & CLKPUT are two other real time clock functions that are implemented on the *PC/+Vs* & *PC/+Vsc*, accessible through INT1AH.

Function	Prior To INT1AH	Upon Return From INT1AH
CLKGET	AH=FEH DL=register* DH=1DH	AL= Value in real time clock register
	<i>*NOTE: register=Specify real time clock register</i>	
CLKPUT	AH=FFH DL=register* DH=1CH AL=value†	No values returned
	<i>NOTES: *register=Specify real time clock register †value=Specify value to go into register</i>	

1.82 Y2K (Year 2000)

BIOS Firmware revision 5.0 or greater is Y2K compliant. It automatically updates the century register in the CMOS RAM.

The BIOS Firmware revision is found in the P.O.S.T Banner of the *PC/+Vs* or *PC/+Vsc*.

1.83 Real Time Clock Memory Map

Register Addresses		Function
Decimal	Hex	
000	00h	Seconds
001	01h	Minutes
002	02h	Hours
003	03h	Day
004	04h	Date
005	05h	Month
006	06h	Year
007	07h	Control
008-015	08h-0Fh	Reserved
016	10h	Floppy Drive Type Byte
017	11h	Reserved
018	12h	Fixed Drive Type Flag Byte
019	13h	Reserved
020	14h	Equipment Byte
021	15h	Base Memory Size (Low Byte)
022	16h	Base Memory Size (High Byte)
023-045	17h-2Dh	Reserved
046	2Eh	Checksum (Low Byte) for registers 10h-2Dh
047	2Fh	Checksum (High Byte) for registers 10h-2Dh
048	30h	Reserved
049	31h	Reserved
050	32h	Reserved
051-058	33h-3Ah	Reserved
059	3Bh	Reserved-LCD Signature
060	3Ch	Reserved-LCD Type
061-63	3Dh-3Fh	Reserved

Note: When using the Direct Edit of the CMOS RAM SETUP, only registers 10h to 3Fh are accessible.

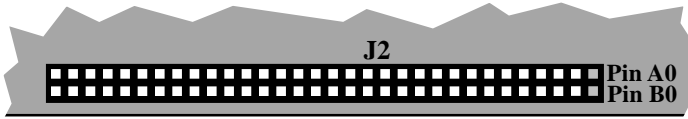
1.90 IBM PC BUS Interface

The IBM PC BUS interface allows many industry-standard I/O modules, which are compatible with the IBM PC BUS bus specification, to be installed on the *PC/+Vs* & *PC/+Vsc*. It provides a quick route for adding a variety of standard I/O functions while keeping the complexity and physical size of the system to a minimum. OEM users who are designing their own special purpose I/O functions may find it convenient to use the IBM PC BUS interface. The pinout of the *PC/+Vs* & *PC/+Vsc* 64-pin PC Bus Header is found in [Table 5.00](#) and the PC Bus Signal Descriptions are found in [Table 5.01](#).

The connector for the IBM PC BUS interface is J2, a 64-pin header with pin A1 through to pin A32, and B1 through to pin B32, corresponding to the PC Bus interface. The IBM PC BUS, bus specification is compatible to the IBM Technical reference manual except as noted below:

1. The Bus clock on the CLK line (pin B20) is a square wave with a frequency of 19.091MHz.
2. The “-12V” line (pin B7), the “+12V” line (pin B9), the “-5V” line (pin B5) and the “/Card Slctd” (pin B8) are not connected on the *PC/+Vs* or *PC/+Vsc* side of the PC BUS. Any cards requiring these voltages would have to have power supplied separately.

Table 5.00 8-bit ISA Bus Header Pinout (J2)



*** WARNING ***

Some of these signals () USED TO BE power pins
These voltages are not connected on the PC/+Vs or PC/+Vsc.*

PC Bus Name	PC/+Vs & PC/+Vsc (J2)	PC/+Vs & PC/+Vsc (J2)	PC Bus Name
GND	A0	B0	+5V
/IOCHK	A1	B1	GND
D7	A2	B2	RESET
D6	A3	B3	+5V
D5	A4	B4	IRQ2
D4	A5	B5	-5V*
D3	A6	B6	DRQ2
D2	A7	B7	-12V*
D1	A8	B8	
D0	A9	B9	+12V*
IORDY	A10	B10	GND
AEN	A11	B11	/MEMW
A19	A12	B12	/MEMR
A18	A13	B13	/IOW
A17	A14	B14	/IOR
A16	A15	B15	/DACK3 [†]
A15	A16	B16	DRQ3 [†]
A14	A17	B17	/DACK1
A13	A18	B18	DRQ1
A12	A19	B19	REFRESH
A11	A20	B20	CLK
A10	A21	B21	IRQ7
A9	A22	B22	IRQ6
A8	A23	B23	IRQ5
A7	A24	B24	IRQ4
A6	A25	B25	IRQ3
A5	A26	B26	/DACK2
A4	A27	B27	TC
A3	A28	B28	ALE
A2	A29	B29	+5V
A1	A30	B30	OSC
A0	A31	B31	GND

Note: This is DMA Channel 3, which utilizes /DACK0 & DREQ0 instead of the usual /DACK3 & DREQ3.

Table 5.01 64-pin 8-bit ISA Bus Pinout (J2)

Symbol	Pin No.	Type	Name and Function
A0-A19	A31-A12	O	CPU Address lines: These lines provide the memory and I/O address for the entire bus cycle. These lines are active high.
D0-D7	A9-A2	I/O	Bi-directional Data Bus: Data is input on these lines during memory, I/O, and interrupt acknowledge read cycles. Data is output on these lines during memory and I/O write cycles. These lines are active high.
+AEN	A11	O	Address Enable: AEN is used to indicate that DMA transfers are taking place. This line is active high. When this line is active, the DMA controller has control of the address bus, the data-bus Read command lines (memory and I/O) and the data-bus Write command lines (memory and I/O).
+IORDY	A10	I	I/O Channel Ready: I/O Channel Ready is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. This line is active high. A low input on this line will insert wait-states into the processor's bus cycle to lengthen I/O or memory cycles so that it may complete its read or write transfer. This line should not be held low for no more than 2.5 microseconds.
/IOCHK	A1	I	I/O Channel Check: -/IOCHK provides the CPU with parity error information regarding the memory or devices using the I/O channel. This signal is active low. When this signal is active, an interrupt is generated to the CPU.
+OSC	B30	O	Oscillator: The OSC is a constant speed 14.31818MHz clock. This signal is not synchronous with the system clock and has a duty cycle of 50%.

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Table 5.01 64-pin 8-bit ISA Bus Pinout (J2) (continued)

Symbol	Pin No.	Type	Name and Function
+ALE	B28	O	Address Latch Enable: This signal is used to latch valid addresses and memory decodes from the microprocessor. When used with AEN, this signal is available to the I/O channel to indicate valid microprocessor or DMA addresses. ALE is an active high signal and microprocessor addresses are latched on the falling edge (high to low) of the ALE signal.
TC	B27	O	Terminal Count: A pulse is put on this line to indicate that the current DMA transfer has reached the terminal count. This signal is active high.
/REFRESH (Generated by the V40H)	B19	O	Refresh: This signal is used to refresh dynamic RAM and can be driven by a microprocessor on the I/O channel. This signal is active low. In the traditional PC/XT architecture this channel is also known as -DACK0. On the <i>PC/+Vs</i> & <i>PC/+Vsc</i> , the V40H outputs this signal.
/DACK1	B17	O	DMA Acknowledge 1 (Spare): -DACK1 is used to acknowledge DMA requests which notifies the individual peripheral it has been granted a DMA cycle. This line is active low.
/DACK2	B26	O	DMA Acknowledge 2 (Floppy): -DACK2 is used to acknowledge DMA requests which notifies the individual peripheral it has been granted a DMA cycle. This line is active low.
/DACK3 (/DACK0 is used here)	B15	O	DMA Acknowledge 2 (Fixed Disk): -DACK3 is used to acknowledge DMA requests which notifies the individual peripheral it has been granted a DMA cycle. This line is active low.

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Table 5.01 64-pin 8-bit ISA Bus Pinout (J2) (continued)

Symbol	Pin No.	Type	Name and Function
+DRQ1	B18	I	DMA Request Line 1(Spare): These lines are individual asynchronous channel request lines input used by peripheral circuits to obtain DMA service. In the traditional XT architecture DRQ1 is unused and DRQ3 is used for a fixed disk controller. These lines are active high.
+DRQ2	B6	I	DMA Request Line 2 (Floppy): DRQ2 is an individual asynchronous channel request input used by the floppy disk controller to obtain DMA service. This line is active high.
+DRQ3 (DRQ0 is used here)	B16	I	DMA Request Line 2 (Fixed Disk): DRQ3 is an individual asynchronous channel request input used by the fixed disk controller to obtain DMA service. This line is active high. On the <i>PC/+Vs</i> & <i>PC/+Vsc</i> , DRQ0 is used.
+IRQ2	B4	I	Interrupt Request 2 (EGA/VGA): IRQ2 is an asynchronous input used to request interrupt service. An interrupt request is executed by raising IRQ2 (low to high) and holding it high until it is acknowledged (edge triggered mode), or holding IRQ2 at a high level until it is acknowledged (level triggered mode). This line is active high. In the <i>PC/+Vs</i> & <i>PC/+Vsc</i> this line is used by the video controller. In the traditional XT/AT architecture this channel is used by LPT2 and some network cards.
+IRQ3	B25	I	Interrupt Request 3 (Com2): IRQ3 is an asynchronous input used to request interrupt service. An interrupt request is executed by raising IRQ3 (low to high) and holding it high until it is acknowledged (edge triggered mode), or holding IRQ3 at a high level until it is acknowledged (level trigger mode). This line is active high. In the <i>PC/+Vs</i> & <i>PC/+Vsc</i> and traditional XT/AT architecture this channel is used by the Com2 port and some network cards.

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Table 5.01 64-pin 8-bit ISA Bus Pinout (J2) (continued)

Symbol	Pin No.	Type	Name and Function
+IRQ4	B24	I	Interrupt Request 4 (Com1): IRQ4 is asynchronous input used to request interrupt service. An interrupt request is executed by raising IRQ4 (low to high) and holding it high until it is acknowledged (edge triggered mode), or holding IRQ4 at a high level until it is acknowledged (level triggered mode). This line is active high. In the <i>PC/+Vs</i> & <i>PC/+Vsc</i> and traditional XT/AT architecture, this channel is used by the Com1 port and some network cards.
+IRQ5	B23	I	Interrupt Request 5 (Spare): IRQ5 is an asynchronous input used to request interrupt service. An interrupt request is executed by raising IRQ5 (low to high) and holding it high until it is acknowledged (edge triggered mode), or holding IRQ5 at a high level until it is acknowledged (level triggered mode). This line is active high. In the <i>PC/+Vs</i> & <i>PC/+Vsc</i> and traditional XT/AT architecture, this channel is used by the fixed disk controller.
+IRQ6	B22	I	Interrupt Request 6 (Floppy Disk): IRQ6 is an asynchronous input used to request interrupt service. An interrupt request is executed by raising IRQ6 (low to high) and holding it high until it is acknowledged (edge triggered mode), or holding IRQ6 at a high level until it is acknowledged (level triggered mode). This line is active high. In the <i>PC/+Vs</i> & <i>PC/+Vsc</i> and traditional XT/AT architecture, this channel is used by the floppy disk controller.
+IRQ7	B21	I	Interrupt Request 7 (Printer Port): IRQ7 is an asynchronous input used to request interrupt service. An interrupt request is executed by raising IRQ7 (low to high) and holding it high until it is acknowledged (edge triggered mode), or holding IRQ7 at a high level until it is acknowledged (level triggered mode). This line is active high. In the <i>PC/+Vs</i> & <i>PC/+Vsc</i> and traditional XT/AT architecture, this channel is used by the parallel printer port (LPT1).

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Table 5.01 64-pin 8-bit ISA Bus Pinout (J2) (continued)

Symbol	Pin No.	Type	Name and Function
CLK	B20	O	Bus Clock: Clock is the processor clock which is a square wave with a frequency of 19.091MHz. <i>Note: Special orders will allow boards to be shipped with the clock equal to half (1/2) the System Clock.</i>
/IOR	B14	O	I/O Read: -IOR instructs an I/O device to place data onto the I/O channel. This signal is active low.
/IOW	B13	O	I/O Write: -IOW instructs an I/O device to read data off of the I/O channel. This signal is active low.
/MEMR	B12	O	Memory Read: -MEMR instructs the memory to place data onto the I/O channel. The signal is active low.
/MEMW	B11	O	Memory Write: -MEMW instructs the memory to read data off of the I/O channel. This signal is active low.
+RESET	B2	O	Reset Drive: Reset Drv indicates that a reset conditon is in progress. This signal is active high and is synchronized to the falling edge of CLK.
+5V	B0, B3 B29	I	VCC: Externally supplied +5V
GND	A0, B1 B10, B31	I/O	GND: Power return of power supply

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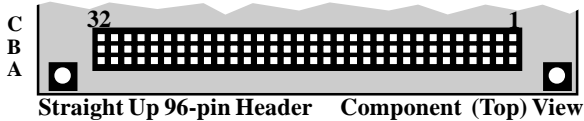
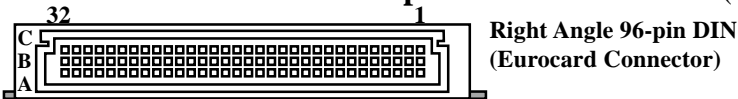
Table 5.01 64-pin 8-bit ISA Bus Pinout (J2) (continued)

****WARNING****

*Some of the following pin assignments are
NO LONGER USED AS POWER PINS*

Symbol	Pin No.	Type	Name and Function
N/C (No longer +12V)	B9	I	Not Connected (+12V): In the traditional XT & AT architecture, this pin is used for +12V. In the <i>PC/+Vs</i> & <i>PC/II+Vsc</i> , this pin is not connected.
N/C (No Longer /Card Select)	B8	---	Not Connected (-Card Select): In the traditional XT & AT architecture, this pin was used for /Card Select or 0WS. In the <i>PC/+Vs</i> & <i>PC/II+Vsc</i> , this pin is not connected.
N/C (No Longer -12V)	B7	O	Not Connected (-12V): In the traditional XT & AT architecture, this pin was used for -12V or unused. In the <i>PC/+Vs</i> & <i>PC/II+Vsc</i> , this pin is not connected.
N/C (No Longer -5V)	B5	I	Not Connected (-5V): In the traditional XT & AT architecture, this pin is used for -5V or unused. In the <i>PC/+Vs</i> & <i>PC/II+Vsc</i> , this pin is not connected.

2.00 96-Pin Eurocard Peripheral I/O Connector (J1)



2.10 PC/+Vs 96-pin Peripheral I/O Connector (J1)

PIN	ROWS		
	A	B	C
1	VID-P3 (SB)	VCC	GND
2	VID-P5 (SR)	VID-P0 (BLUE)	VID-FRM (VSYNC)
3	VID-CSYNC*	VID-P1 (GREEN)	VID-LC (HSYNC)
4	VID-BST	VID-P2 (RED)	VID-ANGREEN
5	VID-M	VID-GND	VID-P4 (INT or SG)
6	VID-ANBLUE	VID-P6 (LD0)	VID-P7 (LD1)
7	VID-ANRED	COM2-RI	COM1-RI
8	VID-/BLA**	COM2-DTR	COM1-DTR
9	SPEAKER	COM2-CTS	COM1-CTS
10	PRN-SLCT	COM2-TXD	COM1-TXD
11	PRN-PE	COM2-RTS	COM1-RTS
12	PRN-BUSY	COM2-RXD	COM1-RXD
13	PRN-AKN	COM2-DSR	COM1-DSR
14	PRN-D7	COM2-DCD	COM1-DCD
15	PRN-D6	COM4-RX	FDD-DCHG
16	PRN-D5	COM4-TX	FDD-HS
17	PRN-D4	KBD-DATA	FDD-RDD
18	PRN-D3	KBD-CLK	FDD-WP
19	PRN-D2	PRN-SELECTIN	FDD-TRK0
20	PRN-D1	PRN-INIT	FDD-WE
21	PRN-D0	PRN-ERR	FDD-WD
22	PRN-STRB	PRN-AUTO	FDD-STP
23	SCSI-D0	SCSI-ATN	FDD-DIRC
24	SCSI-D1	SCSI-BSY	FDD-MD2
25	SCSI-D2	SCSI-AKN	FDD-DS1
26	SCSI-D3	SCSI-RST	FDD-DS2
27	SCSI-D4	SCSI-MSG	FDD-MD1
28	SCSI-D5	SCSI-SEL	FDD-IDX
29	SCSI-D6	SCSI-C/D	FDD-GND
30	SCSI-D7	SCSI-REQ	RESERVED
31	SCSI-DP	SCSI-I/O	FDD-RPM
32	/RESET	VCC	GND

*Note: J1A pin 3 (Csync) can be connected to Vsync or VPBias.

†Note: J1A pin 8 (/BLA) can be connected to Hsync or VPBias.

2.11 *PC/+Vs* Video Interface

The Video Interface on the *PC/+Vs* uses the Vadem® VG-660 VGA LCD Video Controller. This interface is compatible with the IBM-PS2 Video Graphics Array (VGA).

The Video Controller utilizes [IRQ2](#) and has an [I/O address of 3B0h-3DFh](#).

The Video Interface includes a separate 256KByte of Read/Write memory called the “Display Buffer” or “Character generator video RAM”, in which the data to be displayed is stored. The Display Buffer is normally mapped into the CPU’s address space at [0A0000h to 0BFFFFh](#).

2.12 *PC/+Vs* LCD Control

megatel’s *PC/+Vs* provides direct LCD control as an integral part of its on-board video functions. Some of the features, which are part of the Vadem® VG-660 VGA LCD/CRT Controller chip, are as follows:

- 100% IBM VGA compatibility
- Supports lower resolution, small size LCD panels through windowing and panning features
- Provides LCD panel power ON/OFF and sequencing controls
- Directly drives either single or dual screen STN monochrome LCD panels
- Automatic screen centering for short display modes on 480 line monochrome LCD VGA panels
- Supports 16 gray levels in all modes and 64 gray levels in mode 13
- Automatic reduction from RGB color to gray scale and text/background contrast enhancement
- Programmable display output polarity

2.13 PC/+Vs LCD Driver Files

An LCD display is, to the *PC/+Vs* CMOS RAM SETUP, considered a "Special" Display Type. To use an LCD display, a software driver must be used to initialize (or set) the Vadem VG-660 video controller registers to the values which correspond to the display being used.

The *PC/+Vs* BIOS contains Generic LCD Software Drivers, in the form of a Table, that allows many of the popular LCD displays to be used. The "*VG-660 LCD Manual*", formerly entitled the "*PC/+v LCD Manual*", contains our current list of Hex Settings, Panel Manufacturers and Pinouts.

****WARNING****

It is the user's responsibility to check for correctness in pinout.

To implement one of the LCD Software Drivers, one must use the CMOS RAM SETUP*. One of the fields in the CMOS RAM SETUP is the "Display Type". This should be set to "Special" when using an LCD Display. A new field should appear beside the selected "Special" setting. Scroll through this field until you have reached the desired two-digit Hex Setting and be sure to save these settings when exiting the CMOS RAM SETUP.

**Note: See "[1.80 Real Time Clock](#)" chapter for more information regarding the CMOS RAM SETUP.*

Intelligent dot matrix LCD panels do not require the same type of software drivers as do the LCD, EL and Gas Plasma displays. These types of panels are used via the printer port and with an ASCII software program, can output your message etc... .

2.14 PC/+Vs Some Compatible LCD Signal Names

Since there are no “standard” signal names for LCD's, the following table lists some of the compatible signal names used by various panel manufacturers. For a more complete listing of compatible signal names, please read the “*VG-660 LCD Manual*” , formerly entitled the “*PC/+v LCD Manual*”.

PC/+Vs	Sharp	Kyocera	Hitachi	Epson	Matsushita
SCK	CP2; CK; CKD†	CP	CL2; CP	XSCL*	/CLOCK
LC	CPI; LP	LOAD	CL1; LOAD	LP; YSCL*	HSYNC
FLM	S; YD	FRM	FLM	DIN	VSYNC
P0 to P3	UD3 to UD0	HD3 to HD0	UD3 to UD0	UD3 to UD0	DATA-03 to DATA-00
P4 to P7	LD3 to LD0	LD3 to LD0	LD3 to LD0	LD3 to LD0	DATA-E3 to DATAE0
M	M	DF	M; DF	FR	M
/BLANK	H.D; ENAB		DTMG		DISPTMG

**Note: May not always be the case, please refer to the manufacturers specifications.*

†Note: Inverted SCK signal which has to be inverted by user

2.15 PC/+Vs LCD Portion of RTC Memory Map

Register Addresses		FUNCTION
Decimal	Hex	
059	3Bh	Reserved-LCD Signature
060	3Ch	Reserved-LCD Type Flag

2.16 PC/+Vs 96-pin Peripheral I/O: Video Section

VGA VG660 Video Controller with Panels

(see "[PC/+Vs Chart 1](#)", on the next page)

Symbol	Pin No.	Type	Name and Function
P0	B2	O	Panel display data (Bottom screen)
P1	B3	O	Panel display data (Bottom screen)
P2	B4	O	Panel display data (Bottom screen)
P3	A1	O	Panel display data (Bottom screen)
P4	C5	O	Panel display data (Top screen)
P5	A2	O	Panel display data (Top screen)
P6	B6	O	Panel display data (Top screen)
P7	C6	O	Panel display data (Top screen)
M	A5	O	Panel AC signal
FRM	C2	O	Scanning start signal for panel
LC	C3	O	Data latch clock for panel
SCK	A4	O	Shift clock for panel
VIDEO GND	B5	I/O	VIDEO GND: Video Ground

PC/+Vs Chart 1: Interface for Commonly used Panels

The Interface (Pin Assignments) for the most commonly-used Panels are shown below.

Signals Available From PC/+Vs Eurocard Adapter	Signals Available with megatel Video Paddle Board	Mono Single/ Double Screen Panel
P0	P0 (PNL0)	D0
P1	P1 (PNL1)	D1
P2	P2 (PNL2)	D2
P3	P3 (PNL3)	D3
P4	P4 (PNL4)	D4
P5	P5 (PNL5)	D5
P6	P6 (PNL6)	D6
P7	P7 (PNL7)	D7
—	LP0† (PNL8)	—
—	LP1† (PNL9)	—
—	LP2† (PNL10)	—
—	LP3† (PNL11)	—
—	LP4† (PNL12)	—
—	LP5† (PNL13)	—
—	LP6† (PNL14)	—
—	LP7† (PNL15)	—
/BLANK*	/BLANK*	*
CSYNC**	CSYNC**	**
ANGREEN	ANGREEN	—
ANBLUE	ANBLUE	—
ANRED	ANRED	—
SCK	SCK	CL2
M	M	M
FLM	FLM	FLM
LP	LP	LP

Notes:

* This usually has Hsync signal connected.

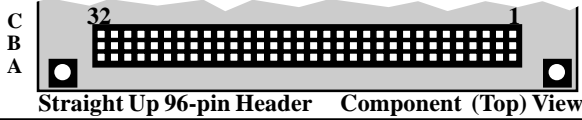
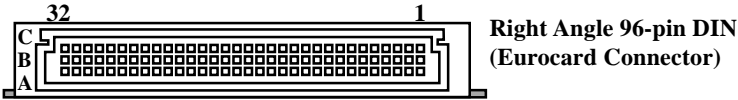
It can be ordered so that VPBias is connected.

** This usually has Vsync signal connected.

It can be ordered so that VPBias is connected.

† These are Latched P0 to P7 signals using SCK active high edge.

2.20 PC/+Vsc 96-Pin Peripheral I/O Connector (J1)



PIN	ROWS		
	A	B	C
1	VID-P3 (SB)	VCC	GND
2	VID-P5 (SR)	VID-P0 (BLUE)	VID-FRM (VSYNC)
3	VID-P8*	VID-P1 (GREEN)	VID-LC (HSYNC)
4	VID-SCK	VID-P2 (RED)	VID-P9 (ANGREEN)
5	VID-M*	VID-GND	VID-P4 (INT or SG)
6	VID-P10 (ANBLUE)	VID-P6 (LD0)	VID-P7 (LD1)
7	VID-P11 (ANRED)	COM2-RI	COM1-RI
8	RESERVED	COM2-DTR	COM1-DTR
9	SPEAKER	COM2-CTS	COM1-CTS
10	PRN-SLCT	COM2-TXD	COM1-TXD
11	PRN-PE	COM2-RTS	COM1-RTS
12	PRN-BUSY	COM2-RXD	COM1-RXD
13	PRN-AKN	COM2-DSR	COM1-DSR
14	PRN-D7	COM2-DCD	COM1-DCD
15	PRN-D6	COM4-RX	FDD-DCHG
16	PRN-D5	COM4-TX	FDD-HS
17	PRN-D4	KBD-DATA	FDD-RDD
18	PRN-D3	KBD-CLK	FDD-WP
19	PRN-D2	PRN-SELECTIN	FDD-TRK0
20	PRN-D1	PRN-INIT	FDD-WE
21	PRN-D0	PRN-ERR	FDD-WD
22	PRN-STRB	PRN-AUTO	FDD-STP
23	SCSI-D0	SCSI-ATN	FDD-DIRC
24	SCSI-D1	SCSI-BSY	FDD-MD2
25	SCSI-D2	SCSI-AKN	FDD-DS1
26	SCSI-D3	SCSI-RST	FDD-DS2
27	SCSI-D4	SCSI-MSG	FDD-MD1
28	SCSI-D5	SCSI-SEL	FDD-IDX
29	SCSI-D6	SCSI-C/D	FDD-GND
30	SCSI-D7	SCSI-REQ	RESERVED
31	SCSI-DP	SCSI-I/O	FDD-RPM
32	/RESET	VCC	GND

*Note: Please see "[2.29 PC/+Vsc 22-pin Jumper Block](#)" chapter

2.21 PC/+Vsc Video Interface

The Video Interface on the **PC/+Vsc** uses the Chips® 65530 Video Controller. This interface is compatible with the IBM-PS/2 Video Graphics Array (VGA) and utilizes [IRQ2](#) and has an [I/O address of 3B0h-3DFh](#).

The Video Interface includes a separate 256KByte* of Read/Write memory called the "Display Buffer" or "Character generator video RAM", in which the data to be displayed is stored. The Display Buffer is normally mapped into the CPU's address space at [0A0000h to 0BFFFFh](#).

**Note: Configurations using 1MByte, instead of the standard 256KByte, is available.*

2.22 PC/+Vsc LCD Control

megatel's **PC/+Vsc** is unique in that it provides direct full panel LCD control as an integral part of its on-board video functions. Some of the features, which are part of the Chips® 65530 video controller chip, are as follows:

- IBM VGA and Register level compatibility.
- Enhanced backward compatibility to EGA™, CGA™, Hercules™, and MDA™ standards
- Interlaced and non-interlaced CRT Displays with resolutions of up to 1024x768 with 16 colors (a resolution of 800x600 with up to 256 colors) can be connected to the **PC/+Vsc**.
- LCD, EL and Plasma panels with resolutions of: 640x200, 640x400, 640x480, 800x600, 1024x768, 1280x1024 can be connected to the **PC/+Vsc**.
- Up to 64-level gray levels on monochrome LCD, EL and gas plasma panels
- Up to 185,193 colors on color TFT LCD, EL and gas plasma panels and up to 226,981 colors on color STN LCD panels.
- A single-screen panel or dual-screen panel (panels that are split into top and bottom halves) can be driven.
- Data can be sent to the panel in parallel 4 bits or 8 bits at a time or in series. 16-bit data can be sent when using the **megatel** Video Paddle Board (a **megatel** cable accessory board, available only upon request).
- Vertical and Horizontal Compensation of displayed text or graphics images on a flat panel.
- SMARTMAP™ intelligent color to gray scale conversion
- Programmable polynomial based Frame Rate Control grey scale algorithm supports fast response "mouse quick" displays by reducing flicker without increasing panel vertical refresh rate.
- Integrated RAMDAC

2.23 *PC/+Vsc* LCD Driver Files

An LCD, EL or Gas Plasma display is, to the *PC/+Vsc* CMOS RAM SETUP, considered a "Special" Display Type. To use one of these displays, a software driver must be used to initialize (or set) the Chips® 65530 video controller registers to the values which correspond to the display being used.

The *PC/+Vsc* BIOS contains Generic LCD Software Drivers, in the form of a Table, that allows many of the popular LCD displays to be used. The "*65530 LCD Manual*", formerly entitled the "*PC/II+ LCD Manual*", contains our current list of Hex Settings, Panel Manufacturers and Pinouts.

****WARNING****

It is the user's responsibility to check for correctness in pinout.

To implement &/or verify the LCD Software Driver, one must use the CMOS RAM SETUP*. One of the fields in the CMOS RAM SETUP is the "Display Type". This should be set to "Special" when using an LCD, EL or Gas Plasma Display. A field should appear beside the selected "Special" setting which should contain the desired two-digit Hex Setting.

**Note: See "[1.80 Real Time Clock](#)" chapter for more information regarding the CMOS RAM SETUP.*

Intelligent dot matrix LCD panels do not require the same type of software drivers as do the LCD, EL and Gas Plasma displays. These types of panels are used via the printer port and with an ASCII software program, can output your message etc... .

2.24 PC/+Vsc Some Compatible LCD Signal Names

Since there are no "standard" signal names for LCD, EL, and Gas Plasma displays, the following table lists some of the compatible signal names used by various panel manufacturers. For a more complete listing of compatible signal names, please read the "*65530 LCD Manual*", formerly entitled the "*PC/II+ LCD Manual*".

PC/+Vsc	Sharp	Kyocera	Hitachi	Epson	Matsushita
SCK	CP2; CK; CKD†	CP	CL2; CP	XSCL*	/CLOCK
LC	CP1; LP	LOAD	CL1; LOAD	LP; YSCL	*HSYNC
FLM	S; YD	FRM	FLM	DIN	VSYNC
P0 to P3	UD3 to UD0	HD3 to HD0	UD3 to UD0	UD3 to UD0	DATA-03 to DATA-00
P4 to P7	LD3 to LD0	LD3 to LD0	LD3 to LD0	LD3 to LD0	DATA-E3 to DATA-E0
P8§	XCLK		R0		
P9 to P11§	R0 to R2		R1 to R3		
M§	M	DF	M; DF	FR	M
/BLANK§	H.D; ENAB		DTMG		DISPTMG

**Note:* May not always be the case, please refer to the manufacturers specifications.

†Note: Inverted SCK. Unless used with the Video Paddle Board, the SCK signal has to be inverted by user.

§Note: Please see the "[2.29 PC/+Vsc 22-pin Video Jumper Block](#)" chapter

2.25 PC/+Vsc LCD Portion of RTC Memory Map

Register Addresses		FUNCTION
Decimal	Hex	
059	3Bh	Reserved-LCD Signature
060	3Ch	Reserved-LCD Type Byte

2.26 PC/+Vsc 96-pin Peripheral I/O: Video Section

VGA 65530 Video Controller with VGA Monitor

Symbol	Pin No.	Type	Name and Function
P11	A7	O	ANRED: Analog Red signal
P10	A6	O	ANBLUE: Analog Blue signal
P9	C4	O	ANGRN: Analog Green signal
FRM	C2	O	VSYNC: Vertical sync signal
LC	C3	O	HSYNC: Horizontal sync signal
VIDEO GND	B5	I/O	VIDEO GND: Video Ground

VGA 65530 Video Controller with EGA Monitor

Symbol	Pin No.	Type	Name and Function
P0	B2	O	BLUE: Primary Blue signal
P1	B3	O	GREEN: Primary Green signal
P2	B4	O	RED: Primary Red signal
P3	A1	O	SB: Secondary Blue signal (Monochrome)
P4	C5	O	SG: Secondary Green signal (Intensity)
P5	A2	O	SR: Secondary Red signal
FRM	C2	O	VSYNC: Vertical sync signal
LC	C3	O	HSYNC: Horizontal sync signal
VIDEO GND	B5	I/O	VIDEO GND: Video Ground

VGA 65530 Video Controller with STN LCD's

(see "[PC/+Vsc Chart 1](#)", on the next page)

Symbol	Pin No.	Type	Name and Function
P0	B2	O	Panel display data (Bottom screen)
P1	B3	O	Panel display data (Bottom screen)
P2	B4	O	Panel display data (Bottom screen)
P3	A1	O	Panel display data (Bottom screen)
P4	C5	O	Panel display data (Top screen)
P5	A2	O	Panel display data (Top screen)
P6	B6	O	Panel display data (Top screen)
P7	C6	O	Panel display data (Top screen)
M	A5	O	Panel AC signal
FRM	C2	O	Scanning start signal for panel
LC	C3	O	Data latch clock for panel
SCK	A4	O	Shift clock for panel
VIDEO GND	B5	I/O	VIDEO GND: Video Ground

PC/+Vsc Chart 1: Interface for Commonly Used Panels

The Interface (Pin Assignments) and settings for CRT's and most commonly used Panels are shown below.

Signals Available From PC/+Vsc Eurocard	Signals Available with megatel Video Adapter	Mono Single Panel	Mono Dual Panel	Color TFT 4-bit	Color STN 4-bit Pack*	Color STN Extended 4-bit Pack*	Color STN DD 16-bit Interface*	CRT Signals‡
P0	P0 (PNL0)	D0	UD3	B0	B2...	R0-G0...	UG1...	BLUE
P1	P1 (PNL1)	D1	UD2	B1	R3...	B0-R1...	UB1...	GREEN
P2	P2 (PNL2)	D2	UD1	B2	G3...	G1-B1...	UR2...	RED
P3	P3 (PNL3)	D3	UD0	B3	B3...	R2-G2...	UG2...	B (VID)
P4	P4 (PNL4)	D4	LD3	G0	R4...	B2-R3...	LG1...	G (INT)
P5	P5 (PNL5)	D5	LD2	G1	G4...	G3-B3...	LB1...	SR
P6	P6 (PNL6)	D6	LD1	G2	B4...	R4-G4...	LR2...	
P7	P7 (PNL7)	D7	LD0	G3	R5...	B4-R5...	LG2...	
---	LP0† (PNL8)	---	UD7	---	R0...	---	UR0...	
---	LP1† (PNL9)	---	UD6	---	G0...	---	UG0...	
---	LP2† (PNL10)	---	UD5	---	B0...	---	UB0...	
---	LP3† (PNL11)	---	UD4	---	R1...	---	UR1...	
---	LP4† (PNL12)	---	LD7	---	G1...	---	LG1...	
---	LP5† (PNL13)	---	LD6	---	B1...	---	LB1...	
---	LP6† (PNL14)	---	LD5	---	R2...	---	LR2...	
---	LP7† (PNL15)	---	LD4	---	G2...	---	LG2...	
P8	P8	---	---	R0	---	SHFCLKU	---	
P9	P9	---	---	R1	---	---	---	ANGREEN
P10	P10	---	---	R2	---	---	---	ANBLUE
P11	P11	---	---	R3	---	---	---	ANRED
SCK	SCK	CL2	CL2	CL2	CL2	SHFCLKL	CL2	
M	M	M	M	M	M	M	M	
FLM	FLM	FLM	FLM	FLM	FLM	FLM	FLM	VSYNC
LP	LP	LP	LP	LP	LP	LP	LP	HSYNC

Notes:

* These are the starting signal names of the "pack".

† These are Latched P0 to P7 signals using SCK active high edge.

‡ Not all of these signals are used at one time.

2.29 PC/+Vsc 22-pin Video Jumper Block

The *PC/+Vsc* has a 22-pin Video Jumper to select LCD or Monitor operation. Ccurrently there is no simultaneous use of LCD's and Monitors.

22-pin Video Jumper Block

LR0	1	2	/ENAVEE/LR0
GND	3	4	/ENAVEE
/BLANK/M	5	6	M
/BLANK	7	8	ANBLUE
LR2	9	10	ANBLUE/LR2
VSYNC/FLM	11	12	FLM
VSYNC	13	14	HSYNC
LP	15	16	HSYNC/LP
LR1	17	18	ANGREEN/LR1
ANRED	19	20	ANGREEN
ANRED/LR3	21	22	LR3

Symbol	Pin	Name & Description
LR0	1	LCD R0 Bit: For LCD use, jumper to pin 2
/ENAVEE/LR0	2	/ENAVEE or LR0 signal: Outputs to J1A pin3
GND	3	Common Ground
/ENAVEE	4	/ENAVEE: For LCD use, jumper to pin 2
/BLANK/M	5	/BLANK or M signal: Outputs to J1A pin 5
M	6	M: For LCD use, jumper to pin 5
/BLANK	7	/BLANK: For LCD use, jumper to pin 5
ANBLUE	8	ANBLUE: For Monitor use, jumper to pin 10
LR2	9	LCD R2 Bit: For LCD use, jumper to pin 10
ANBLUE/LR2	10	ANBLUE or LR2 signal: Outputs to J1A pin 6
VSYNC/FLM	11	VSYNC or FLM signal: Outputs to J1C pin 2
FLM	12	FLM: For LCD use, jumper to pin 11
VSYNC	13	VSYNC: For Monitor use, jumper to pin 11
HSYNC	14	HSYNC: For Monitor use, jumper to pin 16
LP	15	LP: For LCD use, jumper to pin 16
HSYNC/LP	16	HSYNC or LP signal: Outputs to J1C pin 3
LR1	17	LCD R1 Bit: For LCD use, jumper to pin 18
ANGREEN/LR1	18	ANGREEN or LR1 signal: Outputs to J1C pin 4
ANRED	19	ANRED: For Monitor use, jumper to pin 21
ANGREEN	20	ANGREEN: For Monitor use, jumper to pin 18
ANRED/LR3	21	ANRED or LR3 signal: Outputs to J1A pin 7
LR3	22	LCD R3 Bit: For LCD use, jumper to pin 21

2.29 PC/+Vsc 22-pin Video Jumper Block (continued)

Below are some sample jumper settings

22-pin Video Jumper Block

Set for a Monitor (DEFAULT)

LR0	1	2	/ENAVEE/LR0
GND	3	4	/ENAVEE
/BLANK/M	5	6	M
/BLANK	7	8	ANBLUE
LR2	9	10	ANBLUE/LR2
VSYNC/FLM	11	12	FLM
VSYNC	13	14	HSYNC
LP	15	16	HSYNC/LP
LR1	17	18	ANGREEN/LR1
ANRED	19	20	ANGREEN
ANRED/LR3	21	22	LR3

22-pin Video Jumper Block

Set for a color LCD utilizing the /Blank signal as the Display Enable ie. TFT's

LR0	1	2	/ENAVEE/LR0
GND	3	4	/ENAVEE
/BLANK/M	5	6	M
/BLANK	7	8	ANBLUE
LR2	9	10	ANBLUE/LR2
VSYNC/FLM	11	12	FLM
VSYNC	13	14	HSYNC
LP	15	16	HSYNC/LP
LR1	17	18	ANGREEN/LR1
ANRED	19	20	ANGREEN
ANRED/LR3	21	22	LR3

22-pin Video Jumper Block

Set for a color LCD utilizing the M signal ie. STN's

LR0	1	2	/ENAVEE/LR0
GND	3	4	/ENAVEE
/BLANK/M	5	6	M
/BLANK	7	8	ANBLUE
LR2	9	10	ANBLUE/LR2
VSYNC/FLM	11	12	FLM
VSYNC	13	14	HSYNC
LP	15	16	HSYNC/LP
LR1	17	18	ANGREEN/LR1
ANRED	19	20	ANGREEN
ANRED/LR3	21	22	LR3

2.30 Parallel Printer Port

The bi-directional Parallel Printer Port is compatible with the standard PS/2-style printer interface. The IEEE STD1284 standard signaling method for a bi-directional parallel peripheral interface for personal computers is used.

The printer port uses Pins A10 - A22 and B19 - B22 of Eurocard Connector J1 (8 data lines, 5 status inputs, and 4 control outputs).

The status inputs can be read from bits 3 to 7 of [I/O Port 379h](#).

The control outputs are set by writing to Bits 0-3 of [I/O Port 37Ah](#), and can also be read back to determine the actual logic levels on the outputs (as opposed to the logic values written to Port 37Ah). The control lines are open-collector outputs with internal 4.7kΩ pullups.

The eight data bits are written to the latch at [I/O Port 378h](#). Reading Port 378h returns the actual state of the data outputs. The data lines are 3-state TTL outputs.

Bi-directional operation of the Printer Port is achieved by setting Bit 5 of the Control Register (Port 37Ah). When Bit 5 is set (Bit 5=1), the data lines are inputs. When Bit 5 is not set (Bit 5=0), the data lines are outputs.

The interrupt from the Parallel Printer Interface may be disabled under software control, calling IRQ7 to be used on the PC Bus. Clearing Bit 4 of Port 37Ah disables the printer interrupt, while setting Bit 4 enables the interrupt from the printer port. To receive a printer interrupt, [IRQ7](#) must be unmasked in the 8259.

2.31 96-pin Peripheral I/O: Printer Section

Symbol	Pin No.	DB25	Type	Name and Function
SLCT	A10	13	I	Select: Indicates the printer is selected. This signal is active high.
PE	A11	12	I	Paper End: Indicates the printer has sensed the end of paper. This signal is active high.
/BUSY	A12	11	I	Busy: Indicates that the printer is busy and cannot accept data. This signal is active low.
/AKN	A13	10	I	Acknowledge: When active the printer has received the character (data) and is ready to accept another. This signal is active low.
D7, D6, D5, D4, D3, D2, D1, D0	A14, A15, A16, A17, A18, A19, A20, A21	9, 8, 7, 6, 5, 4, 3, 2	I/O	Data Bit 7 to 0: Data is output on these lines to the printer. These lines are active high. On the <i>PC/+Vs</i> & <i>PC/+Vsc</i> , these lines are bi-directional.
STRB	A22	1	O	Strobe: Clocks data to the printer with a 0.5 microsecond (minimum) pulse. This signal is active high. Valid data must be present for a minimum of 0.5 microseconds prior to and after the strobe pulse.
/SELECTIN	B19	17	O	Select in: Selects the printer. This signal is active low.
/INIT	B20	16	O	Initialize Printer: This signal uses a 50 microsecond pulse (minimum) to initialize the printer. This signal is active low.
/ERR	B21	15	I	Error: When this signal is active, it indicates an error has been encountered. This signal is active low.
/AUTO	B22	14	O	Auto Feed XT: When active, it causes the printer to line-feed after a line is printed. This line is active low.
GND	C1/C32	18, 19, 20, 21, 22, 23, 24, 25	I/O	Ground: 0V

2.40 Floppy Disk Interface

The Floppy Disk interface uses the WD37C65 Floppy Disk Controller chip together with custom logic for write data pre-compensation, drive and motor select functions. With the standard BIOS software, one or two double-density, single- or double-sided 5.25-inch or 3.5-inch floppy disk drives can be connected.

[DMA Channel 2](#) is used in conjunction with data transfers between the main memory and the 37C65. The Floppy Disk Controller [I/O address is 3F0h-3F7h](#) with the Floppy Control Port at [I/O address 0FFh](#). The interrupt output from the 37C65 drives [IRQ6](#).

A total of 4 outputs are available for drive select (DSEL) and motor select (MTR) functions. Normally the DSEL0 and DSEL1 outputs (J14-14 and -12) are used to select the drive to be accessed, and MTR0 and MTR1 (J14-10 and -16) enable the spindle motor on the drive.

megatel's BIOS supports all four types of IBM PC drives. You can format the drives as 360kB, 720kB, 1.2MB, or 1.44MB drives. The proper methods of formatting are outlined in the PC DOS, Microsoft DOS and DR DOS manual. Normally the DSEL0 and DSEL1 outputs are used to select the drive to be accessed, and MTR0 and MTR1 enable the spindle motor on the drive. The /RPM output is used to change the spindle motor speed of high density drives to allow the reading of low density media (RPM=1 for 300 RPM in 360kB mode and RPM=0 for 360 RPM in 1.2MB mode).

Notes:

- 1. Some disk drives may have to be reconfigured when used with a twisted cable, different drive speeds and/or whether the drive is used as Drive A or Drive B. Reconfiguration is done by moving the jumpers that are physically on the disk drive. For proper jumper settings, please refer to the manual that came with your drive.*
- 2. The default setting for the "Floppy" option in the CMOS RAM SETUP is for a 3.5" 1.44MB Floppy Disk. This will allow the reading of 720kB, 1.2MB, and 360kB disks—but will not allow formatting to occur. To enable formatting, please set the "Floppy" option in the CMOS RAM SETUP, to the drive size you are using. (See "[1.80 Real Time Clock](#)" chapter for more information regarding the CMOS RAM SETUP)*

2.41 96-pin Peripheral I/O: Floppy Disk Section

Symbol	Pin No.	HDR	Type	Name and Function
/DCHG	C15	34	I	Disk Changed: When active, this signal indicates that the drive door is open or that the diskette has been changed since the last drive selection. This signal is active low.
/HS	C16	32	O	Head Select: This signal selects the head side of the floppy disk that is being read or written. When high it selects side 0 and when low it selects side 1. This signal is active low.
/RDD	C17	30	I	Read Disk Data: When active, this signal reads data from the disk media. Data is read on the falling edge of the encoded data pulse. This signal is active low.
/WP	C18	28	I	Write Protect: This signal senses the status from the disk drive and when active, indicates that the disk is write protected. This signal is active low.
/TRK0	C19	26	I	Track 0: This signal senses the status from the disk drive and when active, indicates when the head is positioned over the track 0. This signal is active low.
/WE	C20	24	O	Write Enable: Just prior to writing on the diskette, this line becomes active to allow current to flow through the write head. This line is active low.
/WD	C21	22	O	Write Data: When active, this signal writes to the disk media. Data is written on the falling edge of the encoded data pulse. This signal is active low.
/STP	C22	20	O	Step Pulse: This signal issues an active pulse to move the drive head from track to track. This signal is active low.
/DIRC	C23	18	O	Direction: This signal determines the direction of the head stepper motor. When this signal is high, the direction is outward. When this signal is low, the direction is inward. This signal is active low.
/MD2	C24	16	O	Motor On Drive 2: When active, drive 2 has its motor enabled. This signal is active low.
/DS1	C25	14	O	Drive Select (Drive 1): When this signal is active, it selects drive 1 to read and write data. This signal is active low.
/DS2	C26	12	O	Drive Select (Drive 2): When this signal is active, it selects drive 2 to read and write data. This signal is active low.
/MD1	C27	10	O	Motor On Drive 1: When this signal is active, drive 1 has its motor enabled. This signal is active low.
/IDX	C28	8	O	Index: This signal senses the status from the disk drive and when active indicates the head is positioned over the beginning of a track marked by an index hole. This signal is active low.
/RPM	C31	2	I	Revolutions Per Minute: Used with dual speed drives. When this signal is active, it reduces the spindle speed from the nominal 360RPM to 300RPM. This signal is active low.
GND	C29	6 & Odd#'s	I/O	Ground: 0V

2.50 SCSI Interface

The SCSI interface utilizes the 5380 SCSI compatible Controller.

The SCSI port uses pins A23 to A30 and B23 to B31 of the 96-pin Eurocard Connector J1.

The SCSI Controller I/O address is 2B0h to 2FFh and DMA 0 (Bus DREQ3). As an option, Interrupt IRQ5 can be connected.

Software drivers are used to enable the use of SCSI hard drives as well as other audio and optical storage devices such as CD Roms.

This SCSI interface is ASPI compatible.

*Note: For more information regarding the software, please refer to the **Read.Me** file on the software diskette.*

2.51 96-pin Peripheral I/O: SCSI Section

Symbol	Pin No.	DB25	Type	Name and Function
/D0, /D1, /D2, /D3, /D4, /D5, /D6, /D7	A23, A24 A25, A26, A27, A28, A29, A30	8, 21, 22, 10, 23, 11, 12, 13	I/O	Bi-directional Data Bus: Data is input on these lines during the I/O read cycle and is output on these lines during an I/O write cycle. These data lines are active low.
/DP	A31	20	I/O	Bi-directional Data Bus Parity: Data parity is odd. This signal is active low.
/ATN	B23	17	I/O	Attention: Indicates an attention condition. This signal is received in the Target role and is driven by an Initiator. This signal is active low.
/BSY	B24	6	I/O	Busy: When active, this signal indicates that the SCSI Bus is being used. It can be driven by both the Initiator and the Target device. This line is active low.
/AKN	B25	5	I/O	Acknowledge: When driven by an initiator, indicates acknowledgement of a -REQ/-AKN data-transfer handshake. As the Target, this signal is received as a response to the -REQ signal. This signal is active low.
/RST	B26	4	I/O	SCSI Bus Reset: When this signal is active, it indicates a SCSI Bus RESET condition.
/MSG	B27	2	I/O	Message: This signal is driven by the Target during the Message phase. This signal is received by the Initiator. This signal is active low.
/SEL	B28	19	I/O	Select: This signal is used by an Initiator to select a Target, or used by a Target to reselect an Initiator. This signal is active low.
/C/D	B29	15	I/O	Control/Data: This signal is driven by the Target and indicates whether Control information or Data information is on the Data Bus. This signal is received by the Initiator. This signal is active low.
/REQ	B30	1	I/O	Request: When driven by a Target, this line indicates a request for a -REQ/-AKN data-transfer handshake. This signal is received by the Initiator. This signal is active low.
/I/O	B31	3	I/O	Input/Output: Driven by the Target, this signal controls the direction of data movement on the SCSI Bus. This signal is also used to distinguish between Selection and Reselection phases. This signal is active low.
GND	C1/C32	7, 9, 14, 16, 18, 24	I/O	Ground: 0V
TERM	—	25	I/O	Terminal Power (+5V via a diode)

2.60 Serial Communications Ports

For the PC/+Vs:

The *PC/+Vs* utilizes a 16C2552 Dual Asynchronous Receiver/Transmitter with FIFO's to provide two full IBM compatible RS-232 serial ports (Com1 and Com2).

The *PC/+Vs* utilizes an ADM211 RS-232 Driver/Receiver along with additional line drivers and receivers to provide RS-232C signal levels. The ADM211 also provides the negative voltage to the drivers.

For the PC/+Vsc:

The *PC/+Vsc* utilizes a 16C2552 Dual Asynchronous Receiver/Transmitter with FIFO's to provide two full IBM compatible RS-232 serial ports (Com1 and Com2).

The *PC/+Vsc* also utilizes two ADM211 RS-232 Driver/Receivers to provide RS-232C signal levels. The receiver for RI2 (Ring Indicator for Com2) is a circuit made up of a 2N3904 and a few resistors.

2.61 Com1: Primary Communications Port

The interrupt from Channel 1 (Com1) drives [IRQ4](#) on the interrupt controller. Com1 can be found at [I/O address 03F8h-03FFh](#).

2.62 Com2: Secondary Communications Port

The interrupt from Channel 2 (Com2) drives [IRQ3](#) on the interrupt controller. Com2 can be found at [I/O address 02F8h-02FFh](#).

The interrupts IRQ3 and IRQ4 can be masked at the interrupt controller.

Note: For other Communication options, such as [Com4](#), please refer to the "[Auxiliary I/O](#)" chapter.

2.63 96-pin Peripheral I/O: Com1 RS-232 Section

Symbol	Pin No.	DE9	Type	Name and Function
/RI	C7	9	I	Com1-Ring Indicator: When this signal is active, it indicates that a ringing signal is being received by the Modem or Data set. This signal is active low.
/DTR	C8	4	O	Data Terminal Ready: When this signal is active, it indicates that the Com port is ready to receive. This signal is active low.
/CTS	C9	8	I	Clear To Send: When this signal is active, it indicates that the remote device is ready to transmit. This signal is active low.
TXD	C10	3	O	Transmit Data (Sout-Serial Output): This signal serially transmits data to the communication link. This signal is set to a logic level 1 upon a Master Reset.
/RTS	C11	7	O	Request To Send: When this signal is active, it indicates that the Asynchronous Communication Element (ACE) is ready to transmit data. This signal is active low.
RXD	C12	2	I	Receive Data (Sin-Serial Input): This signal serially receives data from the communications link.
/DSR	C13	6	I	Data Set Ready: This signal is used by the remote device to indicate that it is ready to establish a link and transfer data with the ACE. This signal is active low.
/DCD	C14	1	I	Data Carrier Detect (RLSD-Receiver Line Signal Detect): When this signal is active, it indicates that the local set has detected a data carrier or signal which meets its signal quality conditions. This signal is active low.
GND	C1, C32	5	I/O	Ground: 0V

2.64 96-pin Peripheral I/O: Com2 RS-232 Section

Symbol	Pin No.	DE9	Type	Name and Function
/RI	B7	9	I	Com2-Ring Indicator: When this signal is active, it indicates that a ringing signal is being received by the Modem or Data set. This signal is active low.
/DTR	B8	4	O	Data Terminal Ready: When this signal is active, it indicates that the Com port is ready to receive. This signal is active low.
/CTS	B9	8	I	Clear To Send: When this signal is active, it indicates that the remote device is ready to transmit. This signal is active low.
TXD	B10	3	O	Transmit Data (Sout-Serial Output): This signal serially transmits data to the communication link. This signal is set to a logic level 1 upon a Master Reset.
/RTS	B11	7	O	Request To Send: When this signal is active, it indicates that the Asynchronous Communication Element (ACE) is ready to transmit data. This signal is active low.
RXD	B12	2	I	Receive Data (Sin-Serial Input): This signal serially receives data from the communications link.
/DSR	B13	6	I	Data Set Ready: This signal is used by the remote device to indicate that it is ready to establish a link and transfer data with the ACE. This signal is active low.
/DCD	B14	1	I	Data Carrier Detect (RLSD-Receiver Line Signal Detect): When this signal is active, it indicates that the local set has detected a data carrier or signal which meets its signal quality conditions. This signal is active low.
GND	C1, C32	5	I/O	Ground: 0V

2.70 Auxiliary I/O

2.71 96-pin Peripheral I/O: Speaker Section

The combination of the [Timer 2 Gate control bit](#) and the [Speaker Data bit](#), allow complex waveforms to be generated on the speaker output.

Symbol	Pin No.	Type	Name and Function
SPEAKER	A9	O	Speaker: This signal comes from a (SPKR) driver circuit and is designed to be used with a Piezo Electric Transducer.
GND	C1/C32	I/O	Ground: 0V

2.72 96-pin Peripheral I/O: Reset Section

This line should be driven with an open-collector or mechanical switch.

Symbol	Pin No.	Type	Name and Function
/RESET	A32	I	Reset: When this signal is in its active state, it results in a hardware reset of the <i>PC/+Vs</i> & <i>PC/+Vsc</i> . This line is active low.

2.73 96-pin Peripheral I/O: Keyboard Section

The keyboard interface is designed to accept a standard XT-compatible or auto-switching serial keyboard. The keyboard port is found at [Port 60h](#) and drives [IRQ1](#). *Note: Pins not listed in the chart below are not connected.*

Symbol	Pin No.	5-pin DIN	6-pin Mini	Type	Name and Function
DATA	B17	2	1	I/O	Bi-directional Serial Data: This is the serial data line for the keyboard.
CLOCK	B18	1	5	I/O	Bi-directional Clock: This is the clock line used to synchronize data transmission from the keyboard to the <i>PC/+Vs</i> & <i>PC/+Vsc</i> .
+5V	B1/ B32	5	4	I/O	Vcc: +5V
GND	C1/ C32	4	3	I/O	Ground: 0V

2.74 Com4

One of the built-in features of the μ PD70208H (V40H™) is a Serial Control Unit which provides a single asynchronous serial channel. On the $PC/+Vs$ & $PC/+Vsc$, it is known as Com4, which is an “always ready” RS-232 serial port.

The $PC/+Vs$ has discreet on-board line drivers and receivers with RS-232C signal levels as well as an ADM211 RS-232 Driver/Receiver, which provides the negative voltage to the discreet drivers.

The $PC/+Vsc$ utilizes the ADM211 for RS-232C signal levels.

The BIOS is programmed to handle the Com4 serial port through standard BIOS Calls (INT 14h) with its protocol lines always ready. *Com4 is not compatible if one talks to the port directly.*

When the V40H /SRDY signal output is enabled, then the Receive Data interrupt from the V40H drives [IRQ2](#).

The I/O Address range for the V40H Serial Port is from [074h to 077h](#).

Overall Note:

Com4 and DMA Channel 3 can not be used simultaneously...please see “[1.40 V40H Serial Port and DMA Channel 3](#)” Chapter.

2.75 96-pin Peripheral I/O: Com4

Symbol	Pin No.	DE9	Type	Name and Function
/RI	—	9	I	Com4 Ring Indicator: This channel indicates that a ring signal is being received by the Modem or Data set. This signal is active low.
/DTR	—	4	O	Data Terminal Ready: When this signal is active, it indicates that the Com port is ready to receive. This signal is active low.
/CTS	—	8	I	Clear To Send: When this signal is active, it indicates that the remote device is ready to transmit. This signal is active low.
TXD	B16	3	O	Transmit Data: This line Transmits Data serially.
/RTS	—	7	O	Request To Send: When this signal is active, it indicates that the Com port is ready to send data. This signal is active low.
RXD	B15	2	I	RS-232 Receive Data: This line Receives Data serially.
/DSR	—	6	I	Data Set Ready: This signal is used by the remote device to indicate that it is ready to send data. This signal is active low.
/DCD	—	1	I	Data Carrier Detect: When this signal is active, it indicates that the local set has detected a data carrier signal. This signal is active low.
GND	—	5	I/O	Ground: 0V

2.80 Other I/O Pinouts & Descriptions

2.81 96-pin Peripheral I/O: Reserved Pins

Symbol	Pin No.	Type	Name and Function
RESERVED	A8	I/O	<i>RESERVED: DO NOT USE</i>
RESERVED	C30	I/O	<i>RESERVED: DO NOT USE</i>

2.82 96-pin Peripheral I/O: Power Supply Section

Symbol	Pin No.	Type	Name and Function
VCC	B1, B32	I/O	+5V: +/-5%
GND	C1, C32 B5, C29	I/O	0V

Note: The voltage Rise Time should be from +2V to +5V within 10ms.

3.00 I/O Addresses

The following is the standard *PC/+Vs* & *PC/+Vsc* I/O Address Map.

Standard I/O Map

Address	I/O Device Function
000 - 00F	8237A
010 - 01F	Reserved
020 - 021	PIC Programmable Interrupt Controller (V40H)
040 - 043	PIT Programmable Interval Timer (V40H)
060 - 06F	Keyboard and System Control
070 - 071	RTC Control and Data Port
072 - 073	Reserved
074 - 077	Serial Port COM 4 (V40H)
078 - 07F	PC Bus
080 - 09F	DMA Page registers
0A0	NMI Mask register
0A1 - 0F7	Reserved
0F8 - 0FE	Aliased
0FF	Floppy Control Port
100 - 177	PC Bus
178 - 17D	Aliased
17E - 2AF	PC Bus
2B0 - 2BF	SCSI Controller
2C0 - 2F7	PC Bus
2F8 - 2FF	Secondary Asynchronous Communications
300 - 377	PC Bus
378 - 37F	Printer
380 - 3AF	PC Bus
3B0 - 3DF	VGA Video Controller (VG660 or 65550)/Printer Adapter
3E0 - 3EF	PC Bus
3F0 - 3F7	Floppy disk interface
3F8 - 3FF	Primary Asynchronous Communications
EFF0-FFFF	V40H

4.00 System Memory Map: With On-Board Video

Memory Address Range (Hex)	Descriptions
<i>Dedicated to On-Board PC/+Vs & PC/+Vsc RAM</i>	
00000-9FFFF	640kB of Read/Write System Memory (0 Wait States)
<i>Allocated to RAM, ROM or PC Bus</i>	
A0000-BFFFF	256kB Video DRAM
C0000-DFFFF	128kB of EPROM Space Enabled to the PC Bus*
E0000-EFFFF	64kB of EPROM Space Enabled to the <i>PC/+Vs & PC/+Vsc</i>
F0000-FFFFF	64kB of megatel System BIOS

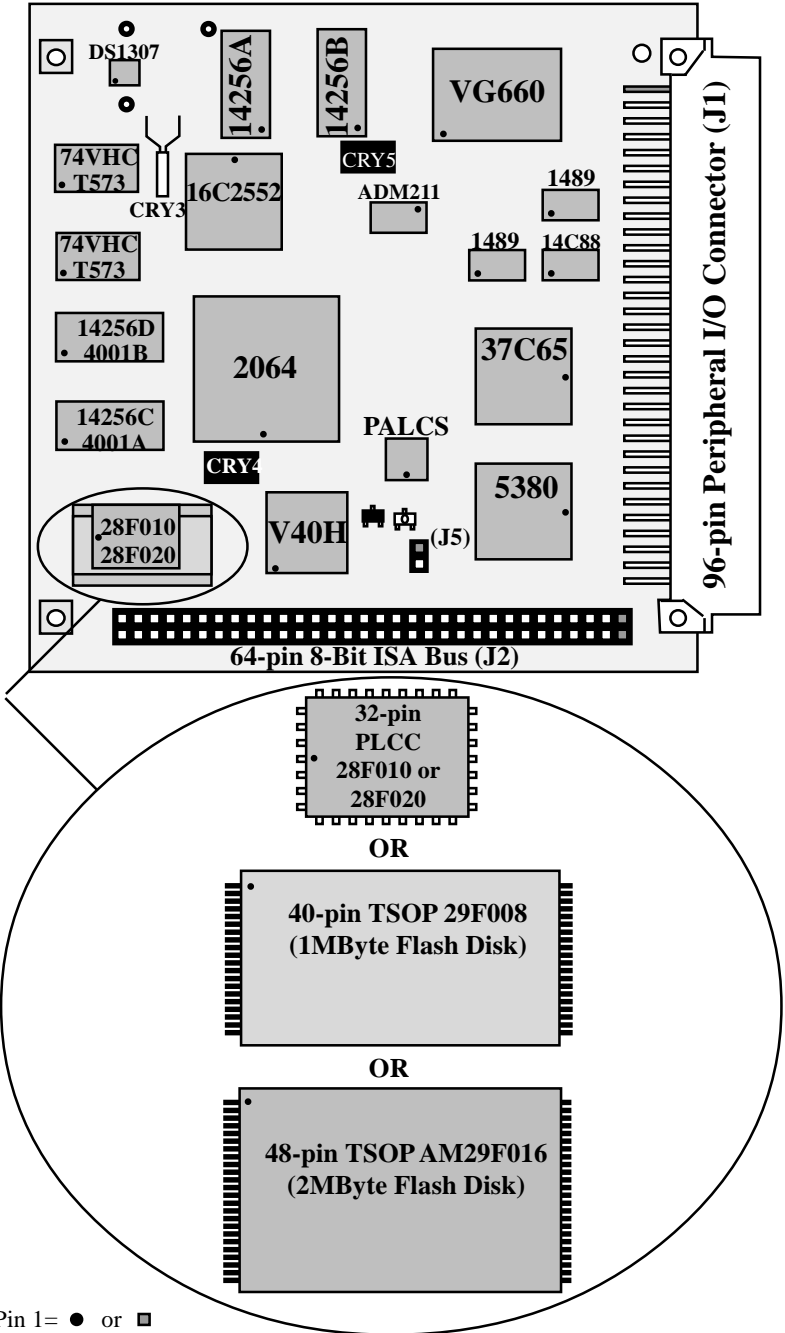
**Note: C0000h to DFFFFh of Address Space can only be enabled to the PC Bus if the 128kB EPROM (28F010) is used.
C0000h to DFFFFh of Address Space is enabled to the 256KB EPROM (28F020) or to the Flash Disk.*

5.00 Parts List, Parts Layout & Mechanicals

5.10 PC/+Vs & PC/+Vsc Parts List (Simple)

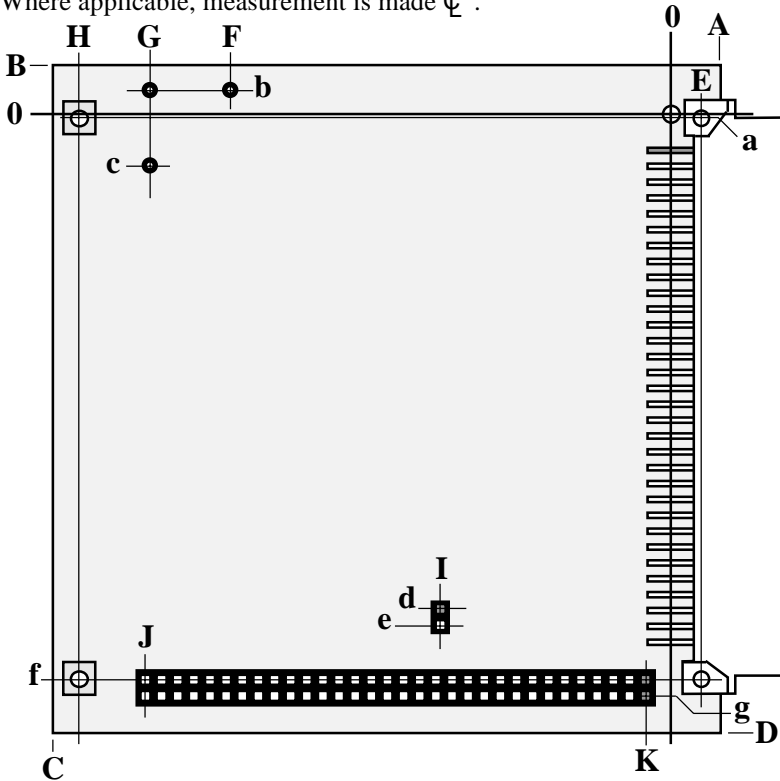
Part Number	Part Description	Location
D: Batt or Batt2	3.0V Lithium Battery (11.05mm spaced) 3.0V Lithium Battery (15.20mm spaced)	BATT or BATT2
I: MT4C4001 or 414256J	1Mx4 DRAM 256Kx4 Video DRAM	U4001A & B U14256C & D
I: 16C2552	Dual Asynchronous UART	U16C2552
I: 14C88	RS-232 Driver (PC/+Vs)	U14C88
I: 1489	RS-232 Receiver (PC/+Vs)	U1489A & B
I: ADM211	RS-232 Drivers/Receivers (PC/+Vs)	UADM211
I: ADM211	RS-232 Drivers/Receivers (PC/+Vsc)	UADM211A UADM211B
I: 2064-70	LCA	U2064
I: 28F010	1Mbit Flash EPROM (128KByte)	U28F010
or 28F020	2Mbit Flash EPROM (256KByte)	U28F020
or E28F008	8Mbit Flash EPROM (1MByte)	U28F008
or 29F016	16Mbit Flash EPROM (2MByte)	U29F016
I: 74VHCT573	Octal D-type Latch (Tri-state)	U573A & B
I: 37C65	Floppy Disk Controller	U37C65
I: 5380	SCSI Controller	U5380
I: VG660	Vadem 660 Video Controller (PC/+Vs)	UV660
I: 65530	Chips® 65530 Video Controller (PC/+Vsc)	U65530
I: MT4C4256	256K x 4 Video DRAM	U14256A & B
or MT4C8512	512K x 8 Video DRAM (PC/+Vsc Only)	U512Kx8A U512Kx8B
I: CY2071A	Video Synthesizer (PC/+Vsc Only)	UCY2071A
I: DS1307	Clock/Calander with 64x8bit SRAM	UDS1307
I: GAL16V8	GAL	UPALCS
I: V40H	CPU	UV40H
J: 2x2 header	Flash EPROM enable/disable jumper	J5
J: 2x32 header or 2x32 socket	PC Bus	J2
J: 3x32 R/A Din or 3x32 header or 3x32 socket	96-Pin Peripheral Connector (R/A DIN)	J1
X: 28.626MHz	Video Synthesizer Crystal (PC/+Vsc Only)	CRY1
X: 32.768KHz	RTC Crystal	CRY3
X: 28.636MHz or 38.182MHz	System Crystal	CRY4
X: 25.175MHz	Video Crystal (PC/+Vs Only)	CRY5

5.20 PC/+Vs Parts Layout



5.21 PC/+Vs Mechanical Specifications

Where applicable, measurement is made C .



A	0.290" (7.37)	a	0.020" (0.508)
B	0.205" (5.21)	b	0.105" (3.81)
C	3.660" (92.96)	c	0.329" (8.36)
D	3.745" (95.12)	d	3.095" (78.61)
E	0.190" (4.826)	e	3.195" (81.15)
F	2.748" (69.80)	f	3.520" (89.41)
G	3.161" (80.29)	g	3.620" (91.95)
H	3.560" (90.42)		
I	1.373" (34.87)		
J	3.210" (81.53)		
K	0.110" (2.794)		

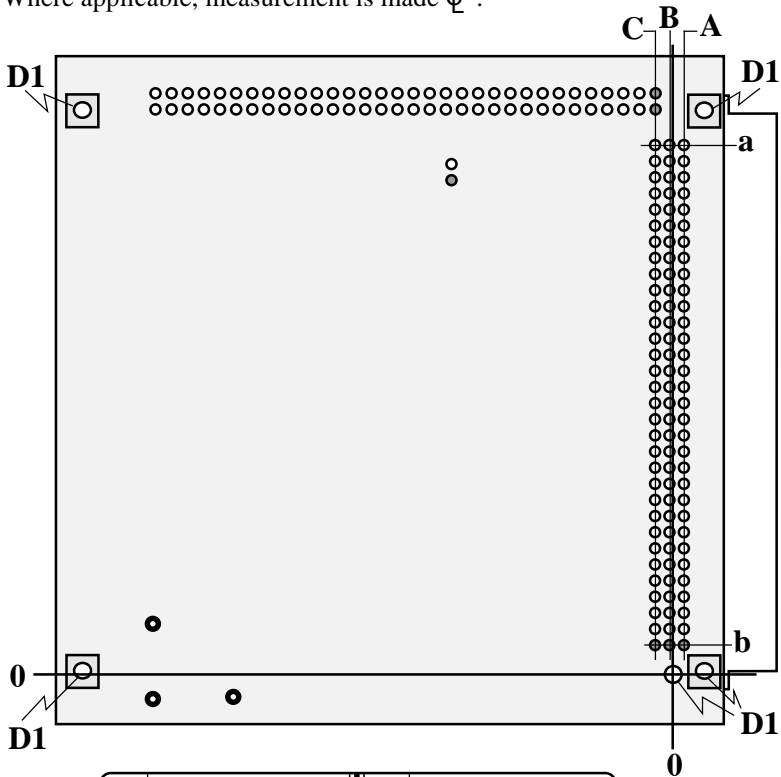
Pin 1= \bullet or \blacksquare

Measurements within () are in mm.

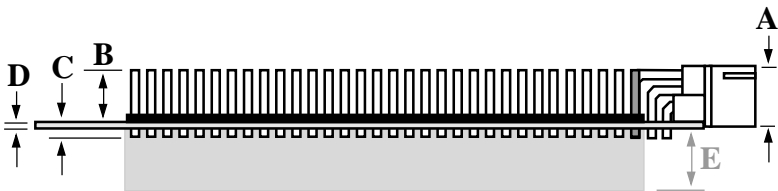
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5.21 PC/+Vs Mechanical Specifications (continued)

Where applicable, measurement is made ϕ .



A	0.090" (2.29)	a	3.320" (84.33)
B	0.010" (0.25)	b	0.220" (5.59)
C	0.110" (84.33)		

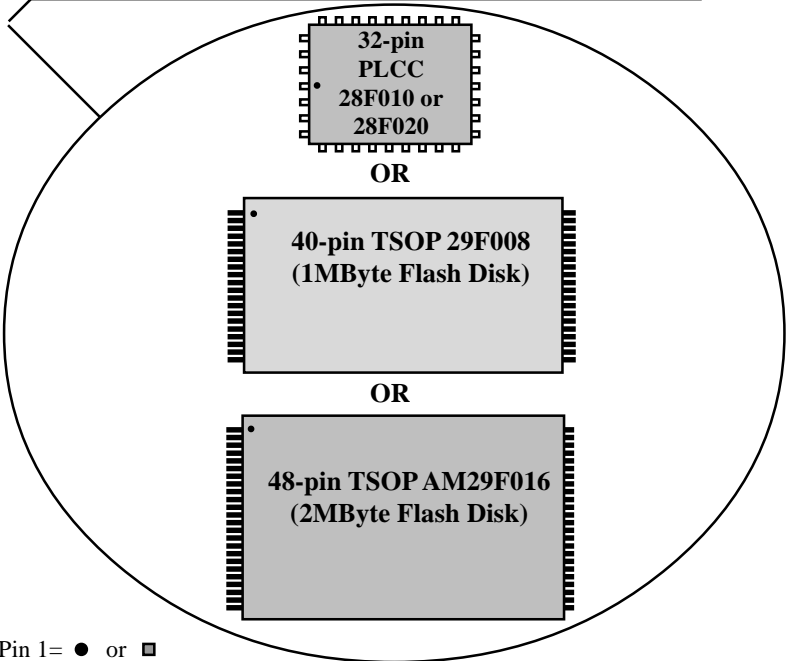
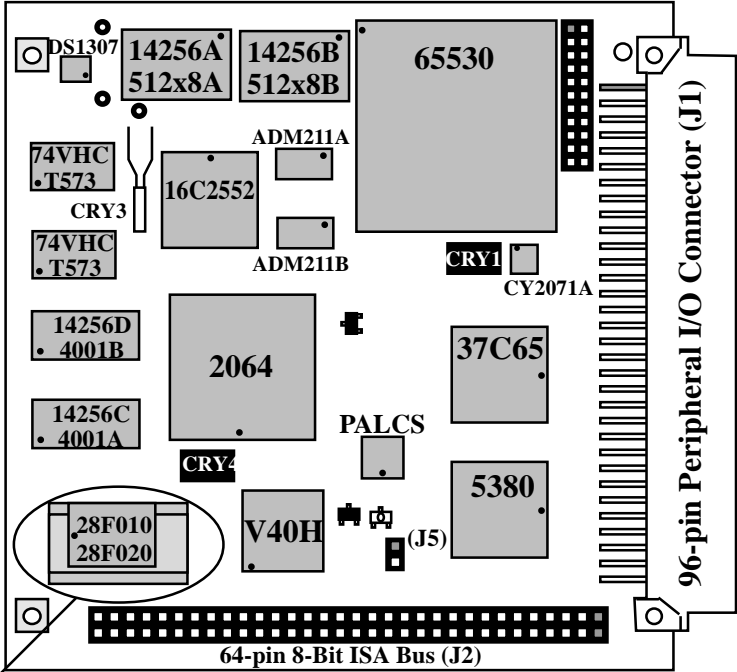


A	0.430" (10.92)	C	0.112" (2.84)
B	0.240" (6.10) (regular header)	D	0.062" (1.57)
	0.410" (10.41) (stack-through)	E	0.435" (11.05) (stack-through)

Pin 1= \bullet or \blacksquare

Measurements within () are in mm.

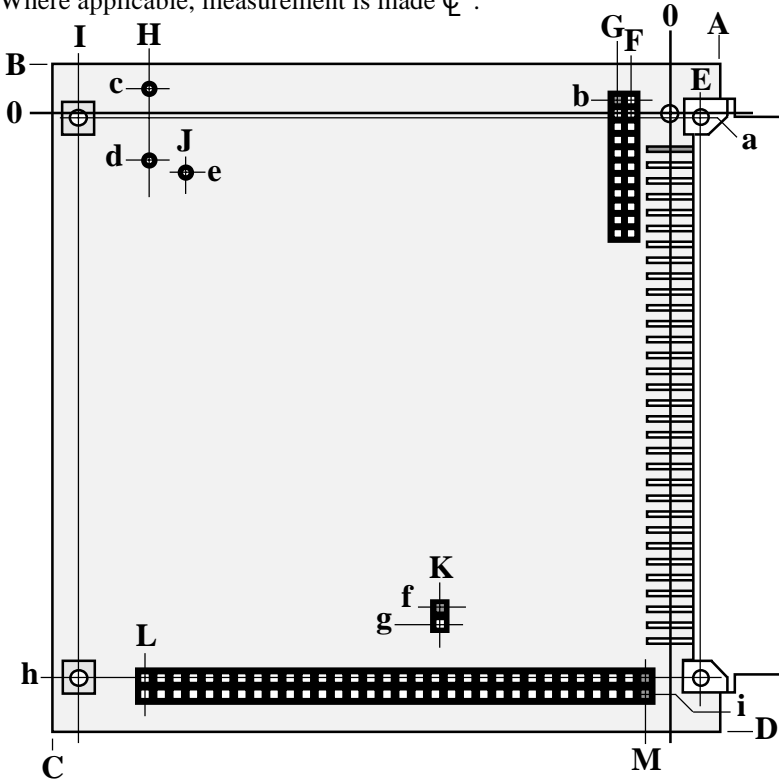
5.30 PC/+Vsc Parts Layout



Pin 1 = ● or ■

5.31 PC/+Vsc Mechanical Specifications

Where applicable, measurement is made \perp .



A	0.290" (7.37)	a	0.020" (0.508)
B	0.205" (5.21)	b	0.080" (2.03)
C	3.660" (92.96)	c	0.094" (2.39)
D	3.745" (95.12)	d	0.340" (8.34)
E	0.190" (4.826)	e	0.458" (11.63)
F	0.206" (5.23)	f	3.095" (78.61)
G	0.286" (7.26)	g	3.195" (81.15)
H	3.198" (81.23)	h	3.520" (89.41)
I	3.560" (90.42)	i	3.620" (91.95)
J	2.963" (75.26)		
K	1.373" (34.87)		
L	3.210" (81.53)		
M	0.110" (2.794)		

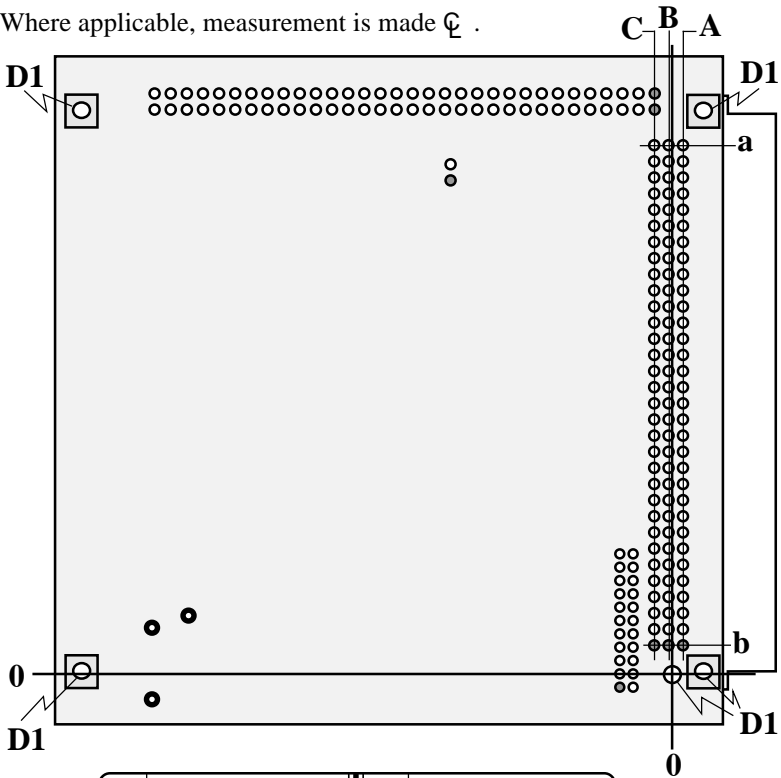
Pin 1= \bullet or \blacksquare

Measurements within () are in mm.

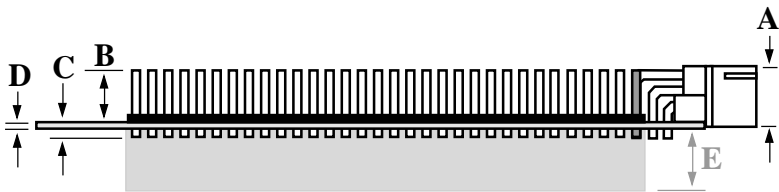
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5.31 PC/+Vsc Mechanical Specifications (continued)

Where applicable, measurement is made \varnothing .



A	0.090" (2.29)	a	3.320" (84.33)
B	0.010" (0.25)	b	0.220" (5.59)
C	0.110" (84.33)		



A	0.430" (10.92)	C	0.112" (2.84)
B	0.240" (6.10) (regular header)	D	0.062" (1.57)
	0.410" (10.41) (stack-through)	E	0.435" (11.05) (stack-through)

Pin 1= \bullet or \blacksquare Measurements within () are in mm.

Notes

6.00 megatel Service Procedure

If you feel your board requires service, **megatel**'s Service Department will do all it can to get you up and running—quickly.

If you purchased your board from our Distributor:

Our Distributors are technically capable to help you get back on track. Since your proof of purchase is from one of our Distributors, you will have to return your board to them. Please follow their instructions for returning your board for service.

If you purchased your board directly from megatel:

Place a Call or Fax to **megatel**'s Service Department **prior to shipping**, to receive your RMA# (Return Materials Authorization Number). Boards that do not have RMA#'s will **not** receive priority. To receive an RMA#, you will be required to provide the following information:

1. Company Name
2. Board Model Number & Serial Number
3. Description of Problem
4. Purchase Order Number

Special Shipping Instructions:

Along with the information requested on the **megatel SERVICE FORM** (follows these shipping instructions), please **include** the following on one of **your** commercial invoices:

1. The value of the board(s)
(this value **must match** the invoice(s) we sent with the board)
2. A copy of the invoice(s) we sent with the boards (Proof of Purchase)
3. Be sure to state **one** of the following:
 - “Canadian Goods Being Returned for Repair”
 - “Canadian Goods Being Returned for Warranty Repair”
 - “Canadian Goods Being Returned”

One copy of the above documents is to be placed **inside** the shipping box and one copy is to be placed on the **outside** of the shipping box (marked for CUSTOMS) Other products (ie. Disk drives, LCD panels, etc...) **which are not** purchased from **megatel**, but will be used as part of the servicing of the returned board, must be shipped separately and listed in the **megatel SERVICE FORM** under the “Equipment Sent Separately” heading. Products **not** purchased from **megatel** should be shipped under a temporary import license of the maximum time limit.

Send **PREPAID** to the SERVICE DEPT. at: **megatel computer corporation**
125 WENDELL AVENUE
WESTON, ONTARIO
M9N 3K9 CANADA
Our Harmonized Number: 8471.92.00

Call us at (416) 245-2953 between the hours of 9am to 5pm EST or send a Fax to us at (416) 245-6505.

...Photocopy and fill in...Photocopy and fill in...Photocopy and fill in...Photocopy and fill...

megatel SERVICE FORM

RMA#: _____ **Call megatel PRIOR TO SHIPPING** to receive your RMA#. Only boards sent with an RMA# will be given priority. This RMA# must appear on all paperwork and be clearly marked on the outside of the shipping box.

Date Called: _____

Company Name: _____

Contact Name: _____

Company Address

Ship To:	Bill To:
_____	_____
_____	_____
_____	_____
_____	_____

Telephone Number: _____ **Extension:** _____

Facimile Number: _____ **Extension:** _____

Fill in the following as completely and as accurately as possible.

Model#	Serial#	Description of Problem

Purchase Order Number for this return: _____

Equipment Sent Separately: _____

(include Model# & Serial#) _____

Courier Used: _____

Waybill Number: _____

Courier Company Name: (Please Circle One)

(Company you wish us to use to return this shipment. Our usual is FED EX)

FED EX EMERY UPS AIR PUROLATOR DHL

BAISLEY OTHER: _____ (If possible)

Special Comments/Instructions you have for us: _____

..Photocopy and fill in...Photocopy and fill in...Photocopy and fill in...Photocopy and fill ...



———— **megatel computer (1986) corporation** ————
——— 125 Wendell Avenue Weston, Ontario Canada M9N 3K9 ———
———— Tel: (416) 245-2953 Fax: (416) 245-6505 ————