Migrating to the PCPi (5V only build) from the PC/II+p

v1.00

This document gives an overview of changes that occur when migrating to the megatel PCPi platform.

Please reference the megatel website (www.megatel.ca) to determine options built on your board, and /or to determine new options available on the PCPi.

The following changes may affect OEM integration of a PCPi in a PC/II+p application (see below for further details):

Connector changes:

1. On Mass IO, IOCS16 signal is grounded on the PCPi;
2. On Mass IO, ACT signal (Flat Panel Activity) is now ground on the PCPi;
3. On Mass IO, ENABKL signal (Enable Backlight) is now reserved;
4. On Mass IO, previously reserved pins now carry signals for COM3, USB3;
5. On Mass IO, ENAVEE signal can be reconfigured to ENABKL (Enable backlight).
6. On Power connector, pins 2,3,4,10 and 11 are now reserved on the PCPi.
7. Ethernet signals are part of an extended Mass IO connector definition.

Other changes:

8. Ethernet is now 10/100BaseT
9. Thermal throttling feature is enabled by default.
10. BIOS Setup editor changes
11. System resource allocations

1. IOCS16 is now grounded

Issue: IOCS16 (pin C28) is now ground on the PCPi Mass IO connector. This signal was connected to IDE drives.

Implication: Originally, the ATA interfaced defined IOCS16 as pulled high at the host, and driven by open-collector drivers by connected drives. Modern ATA controllers no longer require the drive to generate an IOCS16 signal.

Workaround: This signal acts as an additional signal ground, and should be connected to ground if high performance drives are used, or else no action required.

2. ACT signal (Flat Panel Activity) is now grounded

Issue: The flat panel ACT (pin C7) signal has been redefined as ground.

Implication: This status signal was never used by any displays, but may still be driven by older megatel products.

Workaround: If customer application is to be designed to use older megatel products also, this pin should be left as a no-connect. All new megatel products use this pin as an additional signal ground to improve signal integrity, so we recommend this pin be grounded for designs that will not support old megatel products. Check with the factory to determine if older megatel product can be made compatible with this pin grounded.

3. ENABKL (Enable backlight) is now reserved.

Issue: The flat panel ENABKL (pin B7) is reserved.

Implication: This signal should be a no-connect.

Workaround: Use ENAVEE (pin A6, see below) for this function, and contact factory for appropriate BIOS.

4. ENAVEE signal can be reconfigured to ENABKL (Enable backlight).

Issue: The flat panel ENAVEE signal (pin A6) can be reconfigured to carry the ENABKL signal.

Implication: Modern panels do not use a negative supply, so ENAVEE is no longer used.

Workaround: None required.

5. Previously 'reserved' pins now carry signals for COM3, and USB3

Issue: Pins previously marked 'reserved' now carry signals for COM3, and USB3.

Implication: None – these signals were marked 'reserved' on the PC/II+p, but were connected to COM3 header on the megatel QTB-DXP.

Workaround: Ensure that RS232 signals are ONLY applied to RX & TX on the QTB-DXP COM3 header.

6. Power pins 2, 3,4,10 and 11 are now reserved

Issue: Pins 2,3,4,10 and 11 on the power connector are now no connects.

Implication: These pins were defined as 5V supply or key/ground pins on the PC/II+p. Plugging a PCPi into a power connector supplying +5V to these pins may not properly power the board.

Workaround: On boards configured for +5V only supply, ensure sufficient +5V on pins 1&12 only, and ground on pins 5,6,7,8, and 9 only.

7. Ethernet signals are now brought out via an extension of the Mass IO connector

Issue: Ethernet signals are now brought out via an extension of the Mass IO connector. The 2x5 0.100" connector used on the PC/II+p has been removed.

Implication: The 2x5 0.100" Ethernet connector is no longer supported. The AUI interface is no longer supported. If AUI is required, 10BaseT to AUI adapters are commercially available.

Workaround: Boards configured for compatibility with the PC/II+p will be populated with a 5x33 Mass IO connector, and a single 1x5 2mm connector for the Ethernet signals.

8. Ethernet is now 10/100BaseT

Issue: The Intel 82551 (10/100BaseT) Ethernet Controller is provided on the PCPi. Supported drivers can be obtained from:
http://www.intel.com/design/network/drivers/index.html

Implication: No packet driver is available for the Intel 82551. No AUI support.

Workaround: There is a packet driver available for early Intel 10/100 Ethernet controllers, but this has not been tested, and is not expected to work without modifications. If AUI is required, 10BaseT to AUI adapters are commercially available.

9. Thermal throttling is enabled by default

Issue: Thermal throttling is enabled by default. When the sensed (board) temperature reaches 80C, the processor is throttled to a fraction of its normal speed. When temperature drops below 75C, the throttle is released, and the processor is restored to normal.

Implication: If operating in extreme environments where board temperature may exceed the throttle point, system designers must be aware that throttling will significantly reduce system performance.

Workaround: None. Throttling can be disabled, but doing so will have an impact on the system longevity. Throttle threshold temperature can be changed to suit the application. Please contact megatel for support when tailoring thermal throttle to your application.

10. BIOS Setup editor changes

Issue: The BIOS setup editor (commonly called the CMOS editor) has been enhanced to include additional setup pages. Notably, the setup editor now has a "Boot Sequence" page to allow the OEM to select the sequence in which attached media will be tried during boot.

Implication: OEMs may have to enter and alter the default boot sequence to obtain desired operation in their application.

Workaround: Enter the BIOS Setup editor during boot, and edit the boot sequence to your needs. You may then use the EDNVR program (requires DOS) to save an image of the current setup, which EDNVR can then store to other boards.

11. System resource allocations

Issue: The BIOS allocates the following resources to onboard PCI peripherals:

IRQ	IO Range	Memory Range	Device
10	4000-403F	E0000000-E0000FFF	Ethernet
		FE000000-FEFFFFFF	Video
14, 15	F000-F00F		IDE
	8000-803F, 8100-811F		BMU
11		FF000000-FF000FFF	USB

Implication: OEMs may have to alter their own resource allocations to avoid conflict with the above.

Workaround: Avoid using the resources shown above. If this is not possible, megatel may be able to move conflicting resources with a custom BIOS.

Pinout – MASS I/O J904 (Rows A, B, C, D and E) – 5 X 33 2mm HM Connector

33 row build option *(for compatibility with the QTB-DXP)*

PIN GROUP	POS	ROW e	ROW d	ROW c	ROW b	ROW a
L1-PANEL	1	L1-FPD23	L1-FPD22	GND	L1-FPD21	+5V
L1-PANEL	2	L1-FPD20	L1-FPD19	L1-FPD18	L1-FPD17	L1-FPD16
L1-PANEL	3	L1-FPD15	L1-FPD14	L1-FPD13	L1-FPD12	L1-FPD11
L1-PANEL	4	L1-FPD10	L1-FPD9	L1-FPD8	L1-FPD7	L1-FPD6
L1-PANEL	5	L1-FPD5	L1-FPD4	L1-FPD3	L1-FPD2	L1-FPD1
L1-PANEL	6	L1-FPD0	L1-SHFCLK	L1-LP	L1-FLM	L1-ENAVEE
L1-PANEL MS-SPEAKER	7	L1-ENAVDD	L1-M	GND	Reserved	MS-SPKOUT
MR-RESET, MISC K1-KEYBOARD / USB1	8	MR-RSTSW	PWRGOOD	K1-DAT [U1-D-]	K1-CLK [U1-D+]	+3.3V
M1-MOUSE / USB2 P1-PARALLEL1 - LPT1	9	M1-DAT [U2-D-]	M1-CLK [U2-D+]	P1-STB#	P1-AFD#	P1-D0
P1-PARALLEL1 - LPT1	10	P1-ERR#	P1-D1	P1-INIT#	P1-D2	P1-SLIN#
P1-PARALLEL1 - LPT1	11	P1-D3	P1-D4	P1-D5	P1-D6	P1-D7
P1-PARALLEL1 - LPT1 C1-SERIAL1 - COM1	12	P1-AKN#	P1-BUSY	P1-PE	P1-SLCT	C1-DCD
C1-SERIAL1 - COM1	13	C1-DSR	C1-RXD	C1-RTS	C1-TXD	C1-CTS
C1-SERIAL1 - COM1 C2-SERIAL2 - COM2	14	C1-DTR	C1-RI	C2-DCD	C2-DSR	C2-RXD
C2-SERIAL2 - COM2	15	C2-RTS	C2-TXD	C2-CTS	C2-DTR	C2-RI
U3-USB3 C3-SERIAL3 – COM3	16	U3-D-	U3-D+	C3-RXD	Reserved	C3-TXD
CAN-CAN BUS TS-TOUCH SCREEN	17	Reserved	Reserved	Reserved	Reserved	Reserved
TS-TOUCH SCREEN	18	Reserved	Reserved	Reserved	Reserved	Reserved
TS-TOUCH SCREEN U1-USB1 U2-USB2	19	Reserved	U1-D+	U1-D-	U2-D+	U2-D-
F1-FLOPPY1	20	F1-DENSL0#	F1-INDEX#	F1-MTR0#	F1-DS1#	F1-DS0#
F1-FLOPPY1	21	F1-MTR1#	F1-DIR#	F1-STEP#	F1-WDATA#	F1-WGATE#
F1-FLOPPY1	22	F1-TRK0#	F1-WP#	F1-RDATA#	F1-HDSEL#	F1-DKCHG#
V1-VIDEO1 - CRT1	23	V1-R	V1-G	V1-B	V1-HSYNC	V1-VSYNC
A1-IDE1	24	A1-DD7	A1-DD8	A1-DD6	A1-DD9	A1-DD5
A1-IDE1	25	A1-DD10	A1-DD4	A1-DD11	A1-DD3	A1-DD12
A1-IDE1	26	A1-DD2	A1-DD13	A1-DD1	A1-DD14	A1-DD0
A1-IDE1	27	A1-DD15	A1-DMARQ	A1-DIOW#	A1-DIOR#	A1-IORDY
A1-IDE1	28	A1-DMACK#	A1-INTRQ	GND	A1-DA1	A1-DA0
A1-IDE1	29	A1-DA2	A1-CS0#	A1-CS1#	Reserved	Reserved
	30	Reserved	Reserved	Reserved	Reserved	Reserved
	31	Reserved	Reserved	Reserved	Reserved	Reserved
	32	Reserved	Reserved	Reserved	Reserved	Reserved
POWER	33	Reserved	GND	GND	+5V/[NP]	+5V/[NP]

5 Pin Ethernet connector in Mass IO row 36

E0-ETHERNET0		E0-RX-	E0-RX+	E0-LED/CTP	E0-TX+	E0-TX-

NOTE: signals shown with a green background above have changed from the Mass IO defined for the PC/II+p

12-Pin Power connector

1.	+5V
2.	Reserved
3.	Reserved
4.	Reserved
5.	Ground
6.	Ground
7.	Ground
8.	Ground
9.	Ground
10	Reserved
11	Reserved
12.	+5

NOTE: signals shown with a green background above have changed from the power connector defined for the PC/II+p