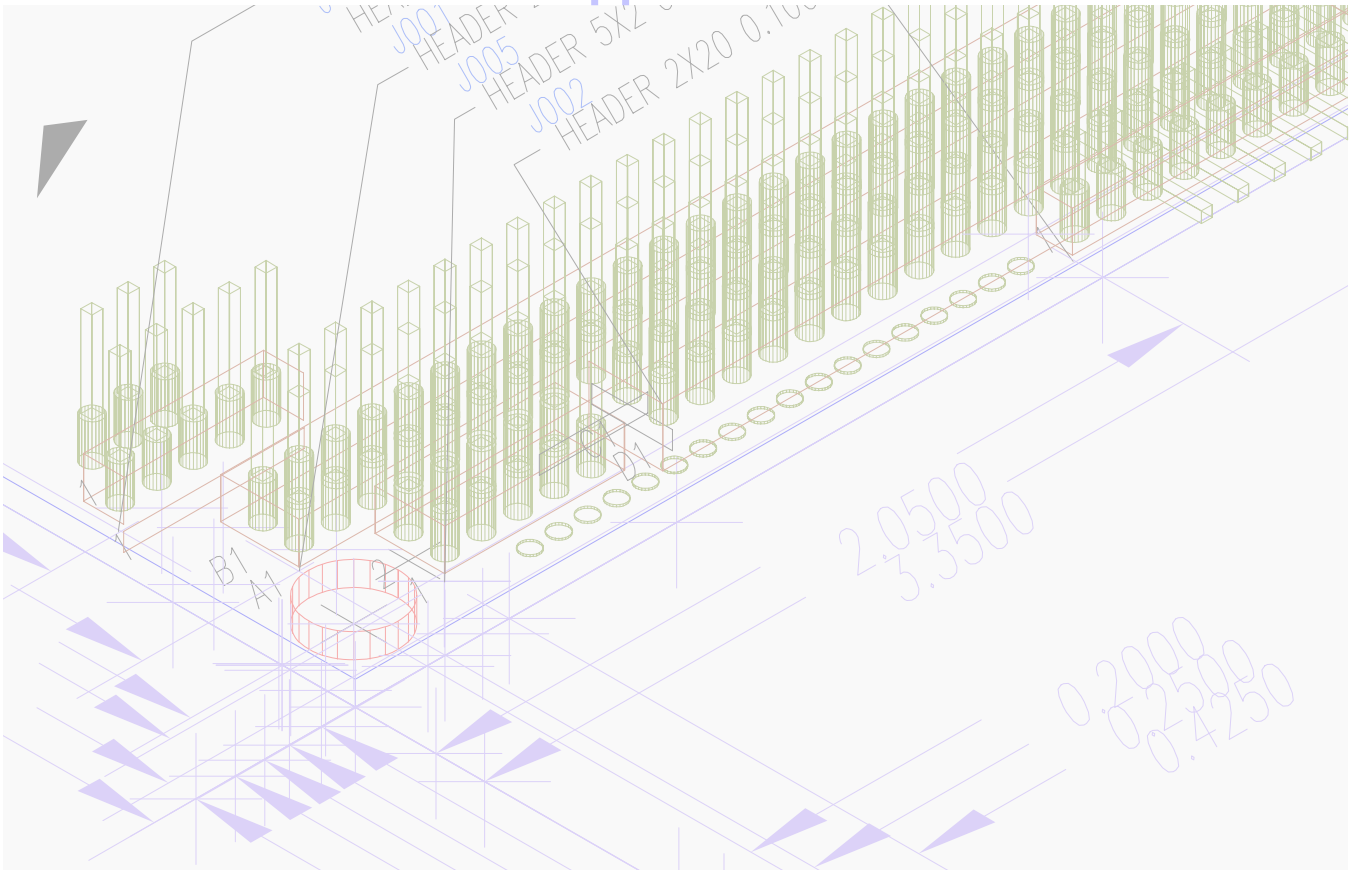
megatel

PC/II+dL

Embedded Modular Computer
for PC/104 Low Power Applications



Technical Reference Manual

Document Number: MT004413
Revision: 1.3
Version: RELEASE

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PC/II+dL

Embedded Modular Single-Board Computer PC/104 Low-Power Applications

megatel 104Family

The ***PC/II+dL*** board is a rugged PC/104 compliant single board computer with all of the features that made us famous. This board is available with a broad set of options that can be mixed in any combination to maximize price and performance. On-board options include DX4 or DX5 processors, Super VGA & LCD output, Ethernet, 2-8MB of soldered-down flash, 4-32MB of soldered-down EDO DRAM, IDE and SCSI. Many other options and base features are packed into this tiny board, all of which are combined into a small rugged package which you will find perfect for your low power applications which require RISC-core DX4/DX5 performance.

Features

- Megatel PC/II+dL Board with Intel DX4 Write-Back Processor, or AMD DX4 Processor, or AMD DX5 Processor, and with National and ACC MICRO super I/O
- Supports 33 MHz FSB and CPU Clocks including 33, 66, 100 and 133 MHz
- 4 MB to 32MB of EDO DRAM soldered down memory
- PC/104 Compliant 16-Bit Bus
- Megatel 104Family-compatible 165-Pin I/O Interface uses IEC 2mm HM Connector System (AMP Z-PACK)
- Crystal CS8900 Ethernet 10Base-T and AUI Controller and Transformers & Filters
- ATA/IDE Hard drive interface
- AT compatible Keyboard and PS/2-Style mouse
- Fast SCSI-2 Interface
- Chips & Tech 65550 CRT and Flat Panel Controller supports both CRT and Flat Panels on a 3.3v or 5v interface
- Quad 16550 Serial Channels support full RS-232 communications
- Parallel Port ECP/EPP (1284 style)
- Floppy Interface, Watchdog, Advanced Y2K Real-Time Clock and all basic AT peripherals
- 256 KB Flash Bios (soldered) for Megatel Custom 100% AT compatible bios and option bios modules
- Flash Disk Disk-on-Chip Socket (up to 144+ MB)
- Soldered Flash Array up to 8 MB
- On-board switching or linear +3.3V supply, or off-board dual +5V and +3.3V supply
- Linux, QNX, DOS, Windows 95/98

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Revision List

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REVISION MT004410a 2000/03/28
PCB version 1.00.

REVISION MT004411 2000/08/18
PCB version 1.01

This version of the PCB incorporates all outstanding ECO's, and adds several options to the board for better control of panels. Minor changes to layout were also made to this version of the board.

Updated Component Bottom Side Diagram for PCB v1.01	26
Updated Features page	3
Electrical Specifications section updated	19,20
Voltage Monitor Specifications updated	22
Component List updated	23
Added Video Linear Buffer Support section	44
Added Option for ENAVEE polarity	93
Updated Product Model Numbering (and Order Information section in general)	89
Updated IRQ table, to indicate PC/104 bus, COMx and Ethernet options separately	56
Added Fan Connector information	32
Added Reset Switch information	39
Added Keyboard & Mouse information	34
Updated pinout sections	Various
Updated QTB/Dxp section for v3.00	87
Updated Memory Map table, for Linear Video Buffer allocation	54
General editing	Various

REVISION MT004412 2000/10/06
PCB version 1.02

This version of the PCB has been finalized for production. Several parts were dual-footprinted to allow population of alternately sourced parts. One redundant option was removed because it was no longer required.

Minimum power requirement updated	15
Electrical Specification updated	19
Absolute Maximum Ratings updated	19
DC Characteristics updated	21
CPU Processor Description updated	27
Order Information updated	89 ff

REVISION MT004413 2001/02/26
PCB version 1.03

This version of the PCB was revised to improve manufacturing and standardize Ethernet options. Except as noted below, functionality, mechanical and electrical interfaces are unchanged.

Notice of new document MT004702, "Ethernet Appbook" added to Ethernet Section	31
Interrupt IRQ Map updated	56
Clarification on the use of the RSTSW# I/O Pin (Manual Reset Switch) Added	20,39,76
Typographic error corrections were also made	Various

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1 Introduction

The Megatel PC/II+dL Cpu board is one of the PC/104 Family Cpu boards from Megatel Computer Corporation. In this document, you will find specifications for the Functional Specifications, Electrical Specifications, and Physical Specifications characteristics of the PC/II+dL Cpu board. Please feel free to contact Megatel or one of its distributors or agents if you require more information.

We have organized this document to present reference material, quick specifications, board settings and electrical specifications. The functional specifications begin in section 6, in topical order, including an introductory parts list and component placement diagrams. We conclude this document with resource maps, connector pinouts and signals, ordering and servicing information. Physical board specifications are placed at the end of the document.

1.1 PC/II+dL Overview

PC/II+dL is a 486 DX4/DX5 based PC/AT® on a PC/104 form factor PCB. It is PC/104 compliant in its form factor and electrical interfaces, including bottom height requirements using basic features of the board. As a member of the Megatel 104Family, it is interchangeable with other members of the family to provide the feature set and performance range you require. The PC/II+dL provides on-board 8-Bit or 16-Bit PC/104 bus connectors to allow direct drop-in compatibility with existing and new PC/104 designs.

PC/II+dL contains an Intel or AMD 486DX4 100 MHz processor with integrated write-back L1 cache that operates at 100 MHz or 66 MHz, or an AMD 486DX5 133 MHz processor that operates at 133 MHz or 100 MHz. An industrial-rated processor is also available for extended temperatures. The local 32-Bit processor bus operates at 33 MHz. An ACC Micro 2089 Chipset provides an ISA Bus bridge, a DRAM memory controller, and a set of standard AT I/O peripherals. The board supports 4 MB, 8 MB, 16 MB or 32 MB of soldered-down EDO DRAM main memory. An onboard CPLD supports the basic functionality of the board. PC/II+dL also contains an on-board Flash Bios and a 100% AT compatible bios. The board contains soldered-down flash array with 2, 4 or 8 MB capacity. In addition, the board contains a socket for Disk-on-Chip to support 2 to 144 MB of M-Systems Flash Disk memory. A rich complement of peripheral controllers and interfaces in included. Full video is provided by the Chips & Tech 65550 controller, supporting simultaneous CRT and a wide variety of 24-Bit flat panels. Both +5V and +3.3V Panels & CRTs are supported. A fast SCSI-2 bus interface is provided. IDE, Keyboard, PS/2-style mouse, and Floppy are provided by the ACC Micro 2089 bus controller. Up to 4 Serial ports are provided by both the ACC Micro 2089 controller and a National 97338 Super I/O, and the board also contains RS232 transceivers for all standard RS232 signals.

All peripheral I/O, including Video CRT, 24-Bit Flat Panel, Keyboard, Mouse, SCSI, IDE, 4 Serial and Parallel ports are pulled to a Mass I/O Connector on the board. The Ethernet is provided separately on a standard 2X5 pin header. A 12-pin power header is provided to supply the single +5V rail to the board and the +5V rail is regulated to +3.3V by a switching or linear on-board power supply; or optionally, +3.3V can also be supplied by a separate 5-pin power header.

Compared to conventional PC/104 Cpu boards, the PC/II+dL provides a very high density solution at a very low cost. The board is offered in its base configuration that consists of minimal memory, system controller and CPU. Any combination of peripherals can be populated at your option to meet your price/performance requirements.

2 Reference Documents

2.1 Datasheets

ACC Micro	ACC 2089 Enhanced Super Chip, Databook, 1997
Adaptec	AIC-6360 Data Book PC-AT to SCSI Host Adapter,
AMD	Enhanced Am486®DX Microprocessor Family, 20736 Rev B Amendment/0, Mar 1997
AMP Incorporated	Catalog 65911, AMP Z-PACK™ 2mm HM Hard Metric Connector System, Sep 1997
Analog Devices	EMI/EMC Compliant ±15 kV ESD Protected RS-232 Line Drivers/Receivers (ADM211E), 1996
Chips and Technologies	65550 (HiQV32™) High Performance Multi-Media Flat Panel / CRT GUI Accelerator, Revision 1.5, Dec 1997 65550 HiQVideo Series Mode Support, 020089-004 (AN89.4), Revision 1.4, Feb 1996
Crystal Semiconductor Corp	CS8900 Highly Integrated Ethernet Controller, DS150PP2, Dec 95
Dallas Semiconductor	DS1706S 3.3V and 5.0V MicroMonitor, Feb 1998
Dallas Semiconductor	DS1685 Real Time Clock, Mar 1998
Intel	Embedded Write-Back Enhanced IntelDX4™ Processor, 272771-002, Dec 1997
Intel	Embedded Intel486™ Processor Family Developer's Manual, 273021
Intel	Embedded Intel486™ Processor Hardware Reference Manual, 273025
Intel	Intel486 Microprocessor Family Programmer's Reference Manual, 240486
Intel	INTEL® StrataFlash™ Memory Technology 32 and 64 Mbits (28F640J5), 290606-006, Jul 1998
National Semiconductor	PC97338 ACPI 1.0 and PC97 Compliant Super I/O, Apr 1998
Valor Electronics Inc.	ST7010 10Base-T Transformer Datasheet, Rev C
Valor Electronics Inc.	Ethernet AUI Transformers (ST7033) Datasheet, E/AUI105-01, Nov 1995

2.2 Reference Standards

PC/104 Consortium	PC/104 specification – Revision 2.3 – June 1996
Annabooks	AT Bus Design IEEE P996-Compatible, Edward Solari
IEEE	P996.1 Standard for Compact Embedded-PC Modules

2.3 Other References

Microsoft Press	The Programmer's PC Sourcebook, Thom Hogan

3 Specification Summary

PC/II+dL Specifications include the following:

- Board form factor
- Board Type
- Architecture (AT)
- Cpu (486 DX4/DX5)
- DMA (7 channels)
- Interrupts (15 Levels)
- Timers/Counters (3)
- PC Speaker
- LEDs (1-3)
- Memory Bus (32-bit)
- Address Bus (32-bit)
- Power Monitor
- Manual Reset
- Memory (EDO DRAM)
- Memory Options (4,8,16,32 MB)
- Keyboard & Mouse (PS/2)
- Printer / Parallel Port (1284)
- Serial RS232 (4)
- SCSI (7 devices)
- IDE (2 devices)
- Video (CRT, 24-bit Flat Panels, 64-bit engine)
- Video Memory (2 MB)
- Flash Array (2-8 MB)
- Flash Disk (Disk-on-Chip™ 16-288 MB)
- Ethernet (10Base-T and/or AUI)
- Floppy Disk (2)
- Real-Time Clock & NV RAM
- Watchdog
- Connectors (Power-12, Power-5, Mass I/O-165, PC/104-104, Ethernet-5)
- Supply Voltage, Power Rating, Regulation, Rise Times
- Storage Temperature
- Operating Temperature
- Software (Operating, Application, BIOS)

3.1 PC/II+dL Board Specifications

Board Form Factor: 3.775 x 3.550 inch, PC/104 compliant
Board Type: FR4
Basic Board Requires: Central Processing Unit
Minimum Memory – Soldered, 4 MB
Minimum Connectors – Power

Architecture: PC/AT
Central Processing Unit: 486DX4 RISC-Core Processor – Intel or AMD
INTEL DX4:
66 MHz and 100 MHz core speed
33 MHz local bus speed
3.3V core and 5V tolerant I/O
32-Bit RISC technology core
Pipelined execution
Integrated Floating-Point unit
Integrated Write-Back or Write-Through Cache
AMD DX4 and DX5:
100 MHz and 133 MHz core speed
33 MHz local bus speed
3.3V core and 5V tolerant I/O
105.6 million bytes/second burst bus
0.35-u CMOS-process technology
Integrated Floating-Point unit
Integrated Write-Back or Write-Through Cache

Cache Memory:	16K of integrated on-chip Cache Memory (L1) Unified organization, uses modified MESI protocol High performance write-back and write-through (user options)
DMA:	(7) Channels, 128 MB addressing
Interrupt Levels:	(15) Standard (2 x 8259A compatible, nested using IRQ2)
Timers/Counters:	AT-compatible
PC Speaker Output:	Yes, Available on Mass I/O connector
LEDs:	(1) System Status (1) Ethernet Link Status (1) Ethernet Activity Status
Memory Bus:	32-Bit
Address Bus:	32-Bit
Power Monitoring:	Dual 5% monitor – 5V rail and on-board 3.3V Reset hold time – 130 ms minimum, 200 ms typical Transient voltage immunity
Manual Reset:	Available on Mass I/O Connector Debounced, generates minimum of 130ms reset on Low to High Initiated by pulling Manual Reset signal line Low, then High
Memory:	EDO DRAM (soldered) memory, 60 ns typical
Memory Options:	4, 8, 16 or 32 MB installed by Option
Keyboard:	PS/2-style Keyboard supported by Mass I/O Connector
Mouse:	PS/2-style Mouse supported by Mass I/O Connector
Printer/Parallel Port:	Full Bi-directional ECP/EPP Parallel Port supported
Serial/RS232 Ports:	(1) to (4) 16C550-compatible Serial Ports 16-byte FIFOs Full EIA-RS232E and CCITT V.28 Transceivers included Output swing ±9V with all Transmitter Outputs loaded with 3K ohms to Ground
Video CRT & Flat Panel:	Chips and Technologies HiQ 65550 GUI Accelerator On-board 2 MB of 60 ns Video EDO DRAM, 512Kx32 Complete Analog CRT Video Interface Complete 24-Bit Flat Panel Interface Monochrome (64 gray scale) or color Hi-Res Passive STN, Active Matrix TFT/MIM LCD, EL Simultaneous CRT / Flat Panel operation supported Local bus interface – 32-Bit 64-bit Graphics Accelerator engine (BitBLT), H/W cursor VGA register set compatibility Supports panels from popular manufacturers such as Sharp, Optrex, Toshiba, Hitachi, Fujitsu, Samsung, NEC, Sanyo and others Chips and Technologies drivers included

ATA/IDE Hard Drives: (2) IDE drives supported

SCSI Bus:
Adaptec AIC6360 Fast SCSI-2 Controller
(7) SCSI-2 devices
Adaptec SCSI BIOS included
Adaptec Drivers also supported
Bootable from either SCSI or IDE drive
Simultaneous use of both SCSI and IDE

Flash Array: Soldered Flash EEPROM – 2, 4 or 8 MB

Flash Disk:
Socket for user-supplied M-Systems On-board Disk-on-Chip solid-state disk – 16 MB to 288+ MB
Coexistence support for both Flash Array and Flash Disk

Ethernet:
Crystal CS8900 High-performance 10Base-T and AUI controller option
IEEE 802.3 compliant MAC engine, full duplex operation
On-chip RAM buffers – for Transmit & Receive frames
AUI port for 10Base-2, 10Base-5 and 10Base-F
10Base-T filters included
10Base-T and AUI isolation transformers are included
10Base-T port has automatic polarity detection and correction
Auto negotiation function
LED for inbound/outbound frames to/from local controller included
LED for either valid 10Base-T link present, or other general function

Floppy Disk:
Integrated Floppy Disk Controller
(2) 3.5" floppy disk drives supported
IBM System 34 double density format (MFM)
Sony EMCA format compatible
Standard transfer rates – 500 Kb/sec, 300 Kb/sec and 250 Kb/sec

Real-Time Clock, Alarm:
Dallas-Certified DS1685 – Y2K Real-Time Clock Controller
Periodic Interrupt Generator – settable to period of from 122 us to 500 ms
Alarm Interrupt Generator – settable to any time of day in 24 hour period
242-byte NVRAM included
12 or 24 hour format
Daylight savings time support
Unique 48-Bit Serial Number can be used for customer application

Watchdog:
Dallas DS1706 Watchdog Timer/Monitor
Defaults at power-on time to software-disabled state
Software enable/disable/strobe is supported
Minimum strobe rate while enabled – 1 strobe/second
Hardware enable/disable jumper option

Connectors:

Power Connector -
(1) standard 1x12 right-angle header, keyed, +5V
(1) standard 1X5 vertical-pin header, keyed, +3.3V
- when "Dual Supply" option ordered
PC/104 Connectors -
(1) 2x32 and (1) 2x20 pin and socket header
stack-through and non stack-through
board stacking is customer specified option
Ethernet Header -
(1) 2x5 right-angle or vertical header
Mass I/O Connectors -
(1) 5x22 and (1) 5x11 2mm HM
total of 5x33 2mm grid
AMP Z-PACK 2mm HM Connector System
Type B22 and C
Support all variations -
straight and right-angle
male and female
Support top mounting (bottom by request)
Support 2mm headers on request (including board stacking headers)
IEC917 and IEC1076-4-101 compliant
All connectors except for the Power header are optional

Peripheral I/O Signals:

Mass I/O Connector and Ethernet Header Signal Pins

Ethernet – 10	Serial COM1 – 8
Floppy – 15	Serial COM2 – 8
IDE – 28	Serial COM3 – 8
Keyboard – 2	Serial COM4 – 8
Mouse – 2	Speaker – 1
Parallel I/O – 17	Video Analog (CRT) – 5
Reset Switch – 1	Video LCD Flat Panel – 32
SCSI – 18	Power & Ground

Supply Voltage:

Single supply at +5V 5%, or
Dual supply at +5V 5% and +3.3V 5%

Supply Power Rating:

Minimum 2.0W-2.5W; Maximum depends upon CPU type & speed & options (excluding external peripheral requirements)

Supply Regulation:

+5V and +3.3V Supplies require regulation to within 5%
+5V Supply maximum rise time (+3V to +5V) required within 100 ms
On-board step-down regulation is provided for the on-board +3.3V supply
On-board power monitor for both 5V rail and on-board +3.3V supplies

Storage Temperature:

-50C to +125C, battery excluded

Operating Temperature:

Commerical 0C to +70C standard
Industrial -20C to +85C available on request
Industrial -40C to +85C available on request

Operating Software:

QNX, Linux, DOS, Windows, Windows 95/98

Application Software:

x86 compatible

Bios Software:

256 KB Flash EEPROM for BIOS
Bios write protection (hardware)
Chips & Technologies 65550 VGA Driver BIOS included
AT compatible BIOS and Architecture

3.2 PC/II+dL Board Block Diagram

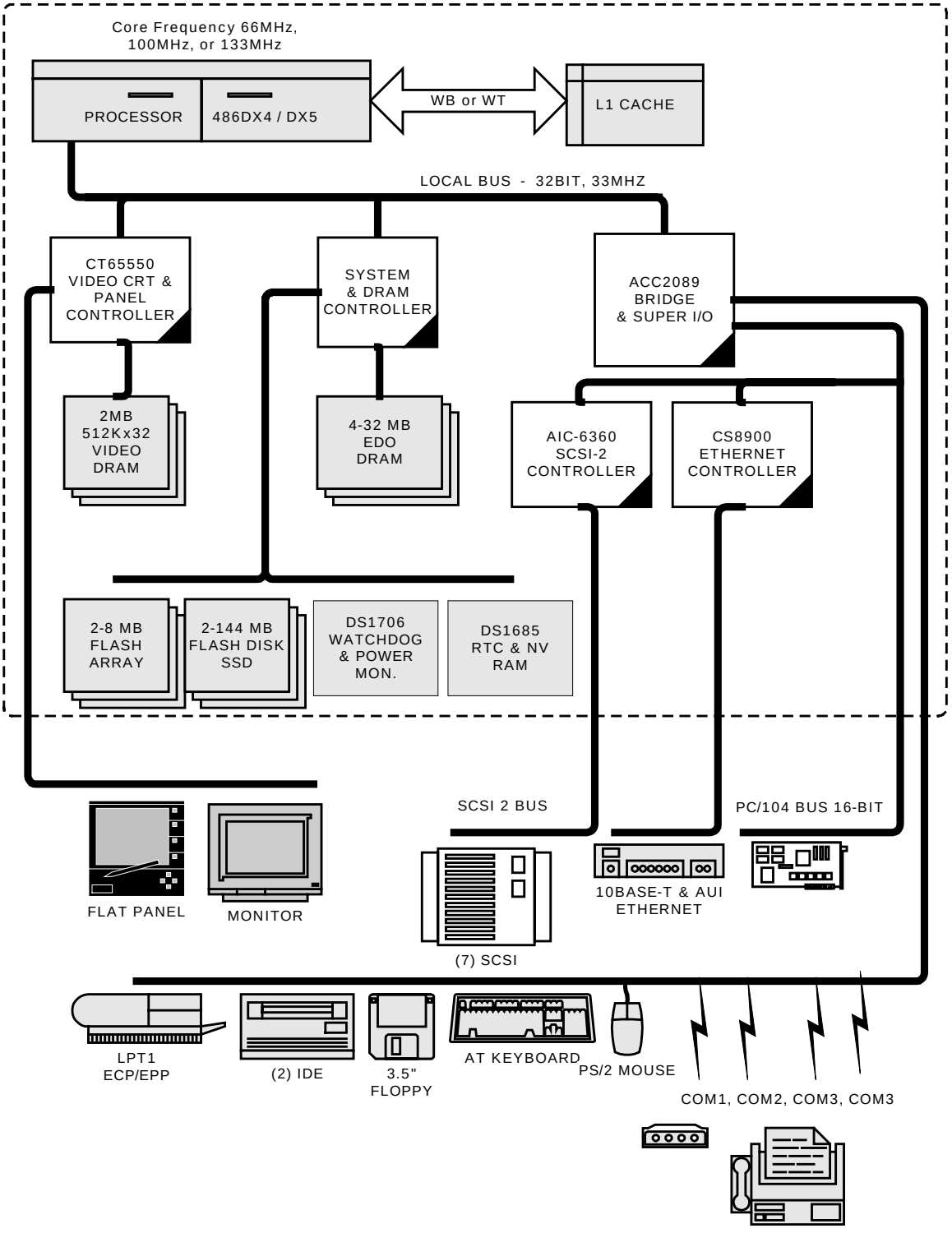


Figure 1 PC/II+dL Block Diagram (v1.03)

4 Settings

4.1 Jumper Settings – User

For position of jumpers, please refer to the Component Placement diagram, section 6.2. All jumpers are *normally* supplied on the TOP side of the board.

Table 1 Jumper Settings – User

JUMPER	SETTING	SELECTED OPTION	COMMENT
JP01	open	Watchdog disabled	(default)
	closed	Watchdog enabled	This option can be ordered; please refer to section 10.3.16. The watchdog controller and its internal functionality will always operate, whether or not this jumper is installed. However, the system will ONLY be forced into reset state at the time of a watchdog timer expiry if the watchdog is enabled by an application program, the timer has expired and this jumper is INSTALLED.
JP02	open	Normal operation	(default) For normal operation, this jumper should be OPEN (no shunt). When the board is powered down, the RTC NV memory is maintained by the battery.
	closed	Reset RTC CMOS memory	Reset RTC. When this jumper is installed as described below, the RTC NV memory is cleared; this allows the BIOS to use its default configuration data rather than the previously saved configuration data when the system is rebooted. 1. This function (Reset RTC) is required to be enabled in the RTC chip; the BIOS provides a call for this purpose. 2. Before closing (installing) this jumper, VCC Power may be present or not present. 3. When the jumper is installed and the function has been enabled by the BIOS, the contents of the RTC NV SRAM User memory (242 bytes used for system configuration) is cleared. 4. The jumper is required to be removed before power is applied. 5. If power is applied when the jumper is installed, remove the jumper and then cycle the power to restore operation. 6. On reboot, default configuration parameters are restored by the BIOS.

4.2 Jumper Settings – Set by Manufacturing

Refer to the PC/II+dx Component Placement diagram. All jumpers are on the TOP side of the board.

Table 2 Jumper Settings – Manufacturing

JP03	open	External bios	Used by Megatel manufacturing only.
	closed	Normal operation	(default) Jumper must be present for normal operation.
JP04	open	Normal operation	(default) Jumper must not be present for normal operation.
	closed	Program bios	Used by Megatel manufacturing only.

5 Electrical Specifications

The PC/II+dL board is powered from either a single +5V ± 5% supply, or from dual +5V ± 5% and +3.3V ± 5% supplies. An on-board switching supply or linear supply may be ordered when the single +5V option is ordered. All boards are shipped with a +5V Power Header (J007), and when a dual supply option is specified, an additional +3.3V Power Header (J010) is also installed on the board.

Megatel recommends using "Dual Supplies" (section 10.3.3, option 3) when available to eliminate the on-board supply for +3.3V. In the case where only +5V is available externally, then Megatel recommends using the on-board Switching regulator supply (section 10.3.3, option 2), which operates typically at an efficiency of above 90% and up to 95%. The board does not require any other supply voltage.

On-board dual voltage monitors are used on all boards.

The PC/II+dL board sources +5V to the PC/104 bus, and can source up to 3.0A @+5V and 50 mA @+3.3V to the MASS I/O connector, for use by optional transition connector boards (transition boards may be supplied directly with external power, or may be designed to utilize power from the PC/II+dL).

5.1 Absolute Maximum Ratings

These specifications apply to the board's physical power connector capabilities and physical board characteristics. Typical specifications can be expected during operation, see sections 5.2 and 5.3, below. Refer to notes below for further information.

Parameter		Symbol	Min	Max	Units	Note
Power Supply Voltage	+5V Digital	VCC5	-0.3	6.0	V	(1)
	+3.3V Digital	VCC3	-0.3		V	(2)
Power Supply Current	+5V (Except Peripherals)	ICC5			mA	(1)
	+3.3V (Except Peripherals)	ICC3			mA	(2)
Ambient Temperature		TA	-55	+125	°C	(3)
Storage Temperature		TS	-65	+150	°C	(3)
Transition Board Current	(+5v To the Mass I/O Connector)	IM5		3000	mA	
	(+3.3v To the Mass I/O Connector)	IM3		50	mA	

Warning: ***Operation at or beyond these limits may result in permanent damage to the board or to components attached to the board. Always operate the board at the Recommended Operating Conditions, see below.***

Warning: ***External +5V and +3.3V power must always be supplied to be board using the appropriate power connector (J007 and J010 respectively). Power must never be sourced to the board using any of the peripheral I/O power pins.***

Note 1. Applies to +5V supplied through the power pins of the POWER connector J007. Connector J007 is ALWAYS populated on the board.

Note 2. Applies to +3.3V supplied through the power pins of the POWER connector J010; Connector J010 is populated when "Dual Supplies" option is ordered. See section 10.3.3.

Note 3. Temperature is given for a board for which power is NOT applied and a Battery is NOT included onboard. If the board contains a lithium battery, then the absolute temperature board ratings must be modified to meet the more restrictive ratings for lithium batteries. Refer to manufacturer's specifications for Lithium Batteries. Never exceed the ratings of a lithium battery if a battery is present on the board.

5.2 Recommended Operating Conditions

The PC/II+dL board is specified to operate within the limits given in this table. In addition to the other limits specified in this document and in manufacturer's documents that are listed in this document, Megatel recommends that you do not operate any parameter given in this table outside of its specified limit range.

Parameter		Symbol	Min	Typical	Max	Units
Power Supply	+5V digital	VCC5	4.75	5.0	5.25	V
	+3.3V digital	VCC3	3.14	3.3	3.46	V
Power Supply Rise Time	+3.0V to +5.0V	VCC5S			100	ms
Operating Ambient Temperature	**(Note 1)**	TA	0		70	°C
Storage Ambient Temperature	**(Note 1)**	TS	-55		+125	°C
Humidity	(Untested)	HA	10		90	% RH
MR-RSTSW# Input Level	Low Level (Note 2)	RSTSWL	-0.03		+0.5	V
	High Level (Note 2)	RSTSWH	+2.8		+3.6	V

NOTES.

(1) Temperature is given for a board for which power IS applied, but a Battery is NOT included. If the board contains a lithium battery, then the absolute temperature board ratings must be modified to meet the more restrictive ratings for lithium batteries. Refer to manufacturer's specifications for Lithium Batteries. Never exceed the ratings of a lithium battery if a battery is present on the board. See Real-Time Clock, sections 6.20 ***and*** 10.3.14***, for more information on the Real-Time clock.***

(2) *Connector J004, pin e8, signal* ***MR-RSTSW#*** *(the RSTSW# input pin) drives the Dallas DS1706 Reset Switch pin. The DS1706 VCC is operated at +3.3V, and therefore* ***the limits specified in the above table apply to the PC/II+dL and must NOT be exceeded****. For compatibility to other Megatel 104Family boards, however, and in accordance with Dallas recommendations, Megatel highly recommends that the RSTSW# line be tied to GROUND to force a reset, and otherwise be left open; in the latter case, an internal 40K resistor in the Dallas DS1706 chip pulls up the Manual Reset Switch pin to a high level during normal operation of the board.*

5.3 DC Characteristics

This table includes the typical operating power requirements for the PC/II+dL board. Because the PC/II+dL board can be ordered with a wide variety of optional components, typical figures are meant to be an indication of expected power, and could be less or more if your options differ from those indicated for this table. You should contact Megatel if you are unsure of what power is used by your configuration of the PC/II+dL board.

Over Recommended Operating Conditions

Parameter		Symbol	Min	Typical	Max	Units	NOTE
Power Supply	+5V (digital)	VCC5	4.75	5.0	5.25	V	
	+3.3V (digital)	VCC3	3.15	3.3	3.45	V	
Power Supply Current	Typical Range	ICC5SW	0.57	1.0		A	1
Power (+5V External, +3.3V External)	Intel DX4 Freq 33 MHz FSB 16 MHz	PDD5A		0.97		W	2
		PDD3A		1.60		W	2

NOTES

(1) Current and power for a typical configuration, assumes single supply with switching regulator. Actual power may be less or more for your specific configuration; please contact Megatel engineering for information on power requirements for specific configurations.

(2) ***Dual Supply Configuration. Both +5V and +3.3V are externally supplied to board. PC/II+dL board contains the following: Intel DX4 CPU operating at specified core frequency and specified local bus frequency, IDE, Floppy Interface, Keyboard & Mouse Ports, 8 MB of EDO DRAM, 4 MB Soldered Flash, and 2 Serial RS232 Ports.***

5.4 Voltage Monitor

An on-board micro voltage monitor is included in the PC/II+dL board. The Dallas Semiconductor DS1706S device provides both a watchdog function and a dual-voltage monitor function. The outputs of the device are directed to the system reset bus, RST and RST#, to provide a system reset at the time of a persistent power exception.

The on-board +3.3V supply rail is monitored at minus 5% by the primary voltage monitor, and the +5V supply is monitored by the IN input voltage sense monitor, using a precision bridge to step the +5V down to the Input Trip Point (1.25V).

Over Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units
+5V Supply Voltage	VCC5	4.75	5.0	5.25	V
+3.3V Supply Voltage	VCC3	3.15	3.3	3.45	V
IN Input Trip Point	VTP	1.20	1.25	1.30	V
VCC5 Trip Point DS1706 NOTE 1	VCC5TP	4.05	4.29	4.53	V
VCC3 Trip Point DS1706	VCC3TP	2.85	2.93	3.00	V
Reset Active Time	TRST	130	205	285	ms
VCC Detect to RST and RST#	TRFP	130	204	285	ms
PBRST# Stable Low to RST *and RST#	TDLY			250	ms
VIN Detect to NMI#	TIPD		5	8	us

NOTES

(1) The +5V supply to the board MUST be externally regulated to produce +5.0V on the board; and if +3.3V is externally supplied, the external supply must be externally regulated to produce +3.3V on the board.

5.5 Bus Drive Current

The PC/104 bus drive current is specified by the PC/104 Specification, Version 1.3, listed in section 2.2. The PC/II+dL board complies to this standard.

Most PC/104 bus signals have a reduced bus drive requirement of 4 mA. The 4 exceptions are open collector driven signals, which must drive 330-ohm pullup resistors defined by the P996 specification.

The following signals must be driven with devices capable of providing 20 mA sink current (all other signals may be driven with devices capable of providing 4 mA sink current):

MEMCS16#, IOCS16#, MASTER# and ENDXFR#.

6 Functional Specifications

6.1 Board Component List

The major components on the PC/II+dL board are contained in the following table. See Notes.

Table 3 Board Component List

REF [3]	QTY	DESCRIPTION [1]	PART [2]	VENDOR
BAT1	1	BATTERY – 3.0V Lithium		
CRY1	1	CRYSTAL – 14.31818 MHz		
CRY2	1	CRYSTAL – 32.768 KHz		
D002	1	LED – Dual Ethernet Activity		
D003	1	LED – System Status		
F001	1	TRANSFORMER – Isolation, Ethernet 10Base-T	ST7010	PULSE
F002	1	TRANSFORMER – Isolation, Ethernet AUI	ST7033	PULSE
J001	1	CONNECTOR – PC/104 2x32 .100 Non-Stack Through Female	ESQ13214GD	SAMTEC
		CONNECTOR – PC/104 2x32 .100 Non-Stack Through Male	EW3209GD-XXX	SAMTEC
		CONNECTOR – PC/104 2x32 .100 Stack Through Female	ESQ13214GD	SAMTEC
		CONNECTOR – PC/104 2x32 .100 Stack Through Male	EW3209GD-XXX	SAMTEC
J002	1	CONNECTOR – PC/104 2x20 .100 Non-Stack Through Female		
		CONNECTOR – PC/104 2x20 .100 Non-Stack Through Male		
		CONNECTOR – PC/104 2x20 .100 Stack Through Female		
		CONNECTOR – PC/104 2x20 .100 Stack Through Male		
J003 [4]	1	CONNECTOR – MASS I/O 5x11 HM 2mm Right-Angle Male	106012-1	AMP
		CONNECTOR – MASS I/O 5x11 HM 2mm Right-Angle Female	100161-1	AMP
		CONNECTOR – MASS I/O 5x11 HM 2mm Straight Male	100159-1	AMP
		CONNECTOR – MASS I/O 5x11 HM 2mm Straight Female	106775-1	AMP
J004 [4]	1	CONNECTOR – MASS I/O 5x22 HM 2mm Right-Angle Male	352131-1	AMP
		CONNECTOR – MASS I/O 5x22 HM 2mm Right-Angle Female	188836-1	AMP
		CONNECTOR – MASS I/O 5x22 HM 2mm Straight Male	352132-1	AMP
		CONNECTOR – MASS I/O 5x22 HM 2mm Straight Female	352268-1	AMP
J005	1	CONNECTOR – ETHERNET, 2X5 .100 Header		
J007	1	CONNECTOR – POWER (+5V), 1x12 .100 Right-Angle Pin Header	22-05-2121	MOLEX
J008	1	HEADER – CPU FAN +5V & GND – 1x2 1.25-mm		
J010	1	HEADER – POWER (+3.3V), 1x5 .100 Straight Male Header		
JP01,JP02 JP03,JP04	4	JUMPER – 1x2 .100 inch		
L006	1	INDUCTOR		
U001	1	CONTROLLER – Bus & DRAM Controller & Super I/O	ACC 2089	ACCMICRO
U002,U003 U006,U007	4	DRAM – EDO, 2MB Memory, 60 ns typical		
U008	1	LOGIC – Gate		
U009	1	LOGIC – Bus Logic	2016	
U010	1	REGULATOR		
U011	1	MONITOR – Power Monitor & Watchdog Controller	DS1706	DALLAS
U013	1	PROCESSOR – Processor, 100 MHz	AM486DX4	AMD
		PROCESSOR – Processor, 100 MHz	FX80486DX4	INTEL
		PROCESSOR – Processor, 133 MHz	AM486DX5	AMD
U016	1	CPLD		

REF [3]	QTY	DESCRIPTION [1]	PART [2]	VENDOR
U021	1	FLASH ROM – ARRAY, 32Mbit (4 MB) Flash	28F320	INTEL
		FLASH ROM – ARRAY, 64Mbit (8 MB) Flash	28F640	INTEL
		FLASH ROM – ARRAY, 16Mbit (2 MB) Flash	28F160	INTEL
U025	1	FLASH ROM – BIOS, 2Mbit (256KB) Flash	29EE020	SST
U028,U029 U031,U032	4	TRANSCEIVER – RS232 ESD Transceivers	ADM211E	ANALOG
U030	1	SUPER I/O	PC97338	NATIONAL
U033	1	SCSI – SCSI-2 Controller	AIC6360	ADAPTEC
U034	1	ETHERNET – Ethernet Controller	CS8900	CRYSTAL
U035	1	ETHERNET – Configuration EEPROM	92C46	
U036	1	VIDEO – Video CRT/Flat Panel Controller	65550	CHIPS
U037	1	DRAM – VIDEO, EDO, 2MB Memory, 512Kx32		
U038	1	LOGIC – Gate		
U039	1	LOGIC – Gate		
U040	1	SOCKET – DIP 32, for M-Systems Disk-on-Chip Flash Disk	238242-4	AMP
U041	1	CLOCK – Quad Programmable Clock Generator		
U042	1	LOGIC – Gate		
U043	1	RTC – Real-Time Clock	DS1685	DALLAS
U044	1	LOGIC – Gate		
U049	1	REGULATOR – Switching		
U050	1	LOGIC – Bus Switch		
U051	1	LOGIC – Bus Switch		
U052	1	LOGIC – Inverter		

NOTES

[1] For component specifications, refer to the applicable data sheets from the component respective manufacturer.

[2] All part numbers are generic, and boards may be shipped with alternatively-sourced parts which are functionally equivalent. If substitution of parts is required by Megatel, Megatel will make every attempt to provide a functionally equivalent parts, and Megatel reserves the right to change any component on the board (for example, if a component becomes obsolete, a second source part may be substituted). Please contact your distributor or agent, or contact Megatel directly if you have specific component requirements.

[3] Parts may or may not be populated on any given board depending upon the board's particular configuration.

[4] Connectors J003 and J004 can be populated with a variety of connector arrangements including straight 2-mm headers and sockets, and right-angle male and female connectors.

6.2 Component Placement – Top Side

The following diagram shows the components on the top (component) side of the PC/II+dL board.

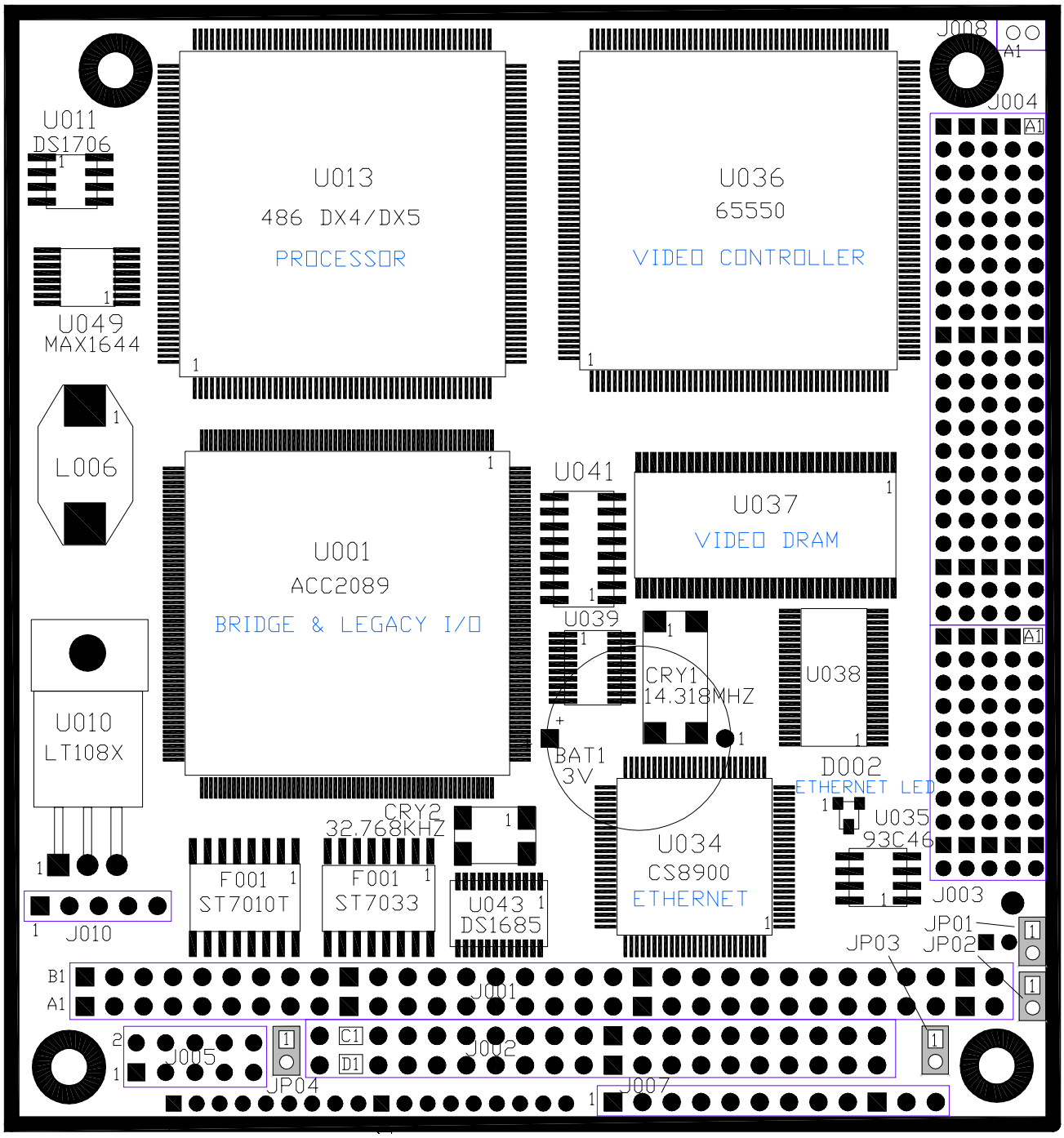


Figure 2 Component Placement – Top Side (v1.03)

6.3 Component Placement – Bottom Side

The following diagram shows the components on the bottom (solder) side of the PC/II+dL board.

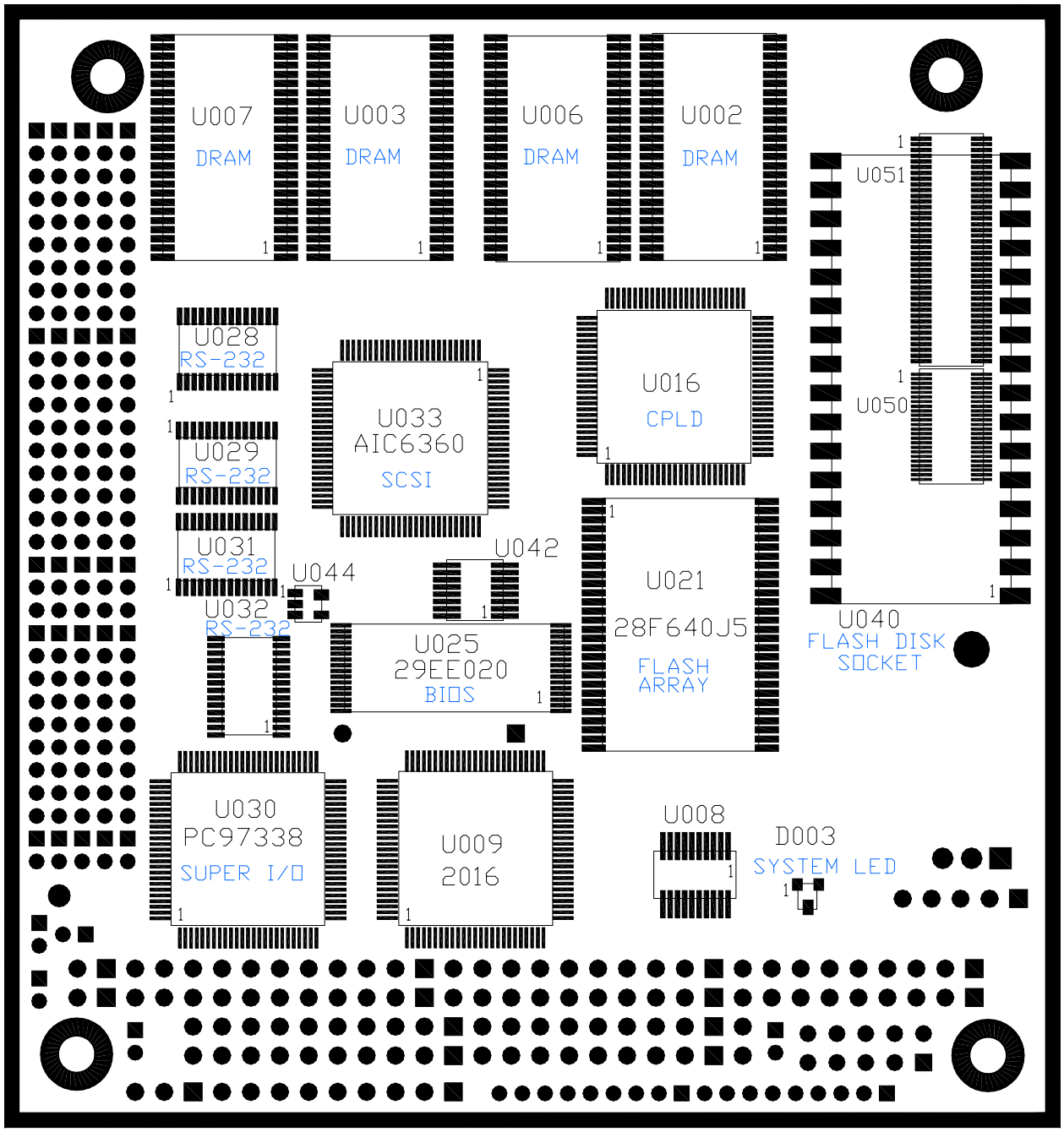


Figure 3 Component Placement – Bottom Side (v1.03)

6.4 Cpu Processor

PC/II+dL is shipped with a user-selected Intel DX4 or AMD 486DX4/DX5 Processor installed.

The PC/II+dL can be shipped with a commercial processor – an AMD 486 DX5 133 MHz processor, an Intel 100 MHz 486 processor, an AMD 100 MHz 486 processor, or an Intel 66 MHz 486 processor. An industrial processor is also available. The Intel DX2 33 MHz can also be shipped for low power applications. All standard operating software such as Linux, QNX, DOS, Windows, Windows 95/98 are supported.

Table 4 Processor Options

Code	Processor	Freq	Ratio	Rating
1	Intel DX4 100 MHz	100 MHz	3:1	Commercial
2	AMD DX4 100 MHz	100 MHz	3:1	Commercial
3	AMD DX5 133 MHz	133 MHz	4:1	Commercial
4	Intel DX4 66 MHz	66 MHz or 33 MHz	3:1	Commercial
5	AMD DX4 100 MHz Ext	100 MHz	3:1	Industrial

NOTE 1. Please contact Megatel for the latest processor options before finalizing any design.

The 486 DX4/DX5 processor is a full 32-bit pipelined RISC Core, with integrated Floating-Point and Write-Back or Write-Through Cached memory. It provides a high level of performance combined with a low cost base and a rich set of features and Industry Standard 486/386 Compatibility.

All DX4 and DX5 processors support host local bus speeds at 33 MHz, providing burst I/O transfers in excess of 100 Million bytes/second. Core frequencies of DX4 processors are 66 MHz or 100 MHz, and of DX5 processors are 100 MHz or 133 MHz. Performance is greatly enhanced by the inclusion of Enhanced bus mode which provides the capability to support Write-back caching. Either Write-back or write-through caching is a selectable option. All processors implement 16K cache on-chip to provide very fast memory access for both frequent memory accesses to code and/or data. The cache is controlled using a modified MESI protocol, and the cache is implemented as a 'unified' cache to maximize hit ratios when code-to-data ratios are skewed.

The 486DX family processors support all x86 operating modes, including real mode, native protected mode and virtual mode, and support the full x86 instruction sets, register sets, memory management and I/O management functions. Many frequently-executed instructions take 1 cycle, and pipe-lined architecture allows multiple instructions to execute concurrently. An integrated on-chip floating-point unit supports the full Intel floating-point instruction set and data type set and provides high data rates.

All peripheral controllers are provided on-board as standard options. Any mix of options can be ordered, which results in a board with the exact price/performance you require.

For Processor order option, see section 10.3.11.
For Cache memory description (L1 cache within the processor chip), see section 6.6.
For the Intel DX4 in DX2 mode (33 MHz core, 16 MHz FSB), contact Megatel or your representative.

6.5 Bus, DRAM Memory, Peripheral Controller

PC/II+dL is shipped with a highly-integrated ACC Micro ACC 2089 controller. This controller implements the PC/104 (ISA) bus control functionality by bridging the local bus to the PC/1104 bus. It also supports a full memory controller function, and provides standard AT architectural functions. A set of integrated peripheral I/O controllers is also provided.

A description of the various functions of this controller are found in summary form in the corresponding sections of this document. For more detailed specifications, please refer to the ACC 2089 datasheet found in the section 2.1.

6.6 Cache Memory

Performance is greatly enhanced by the inclusion in the DX4 and DX5 of Enhanced bus mode which provides the capability to support Write-back caching. Either Write-back or Write-Through caching is an order option (section 10.3.1). All processors implement 16K cache on-chip to provide very fast memory access for both frequent memory accesses to code and/or data. The cache is controlled using a modified MESI protocol, and the cache is implemented as a 'unified' cache to maximize hit ratios when code-to-data ratios are skewed.

6.6.1 Write-through (WT)

Writes and reads to and from system memory are cached. Reads come from cache lines on cache hits; read misses cause cache fills. Speculative reads are allowed. All writes are written to a cache line (when possible) and through to system memory. When writing through to memory, invalid cache lines are never filled, and valid cache lines are either filled or invalidated. This type of cache-control is appropriate for frame buffers. Write-Through is required when there are devices on the system bus that access system memory, but do not perform snooping of memory accesses. It enforces coherency between caches in the processors and system memory.

6.6.2 Write-back (WB)

Writes and reads to and from system memory are cached. Reads come from cache lines on cache hits; read misses cause cache fills. Speculative reads are allowed. Write misses cause cache line fills (in the P6 family processors), and writes are performed entirely in the cache, when possible. The write-back memory type reduces bus traffic by eliminating many unnecessary writes to system memory. Writes to a cache line are not immediately forwarded to system memory; instead, they are accumulated in the cache. The modified cache lines are written to system memory later, when a write-back operation is performed. Write-back operations are triggered when cache lines need to be de-allocated, such as when new cache lines are being allocated in a cache that is already full. They also are triggered by the mechanisms used to maintain cache consistency. This type of cache-control provides the best performance, but it requires that all devices that access system memory on the system bus be able to snoop memory accesses to insure system memory and cache coherency.

If you are unsure of which option to order, contact your representative or Megatel Engineering. Write-back provides the best performance, but requires (a) all system bus devices to use bus snooping, and (b) no real-time semaphore coherency problems exist in your applications. Write-through will always be acceptable for all bus devices and applications.

For Cache order option information, see section 10.3.1.

6.7 Connectors

The following connectors are available (by option, except for J007 which is required):

- J001 – PC/104 Connector "AB" – 2x32 (.100 inch pitch) pinout, section 8.1
- J002 – PC/104 Connector "CD" – 2x20 (.100 inch pitch) pinout, section 8.1
- J003 – Mass I/O Connector – 5x11 (2-mm HM pitch) pinout, section 8.2
- J004 – Mass I/O Connector – 5x22 (2-mm HM pitch) pinout, section 8.2
- J005 – Ethernet Header – 2x5 (.100 inch pitch) pinout, section 8.3
- J007 – +5V Power Header – 1x12 (.100 inch pitch) pinout, section 8.4
- J008 – Fan Connector – 1x2 (1.25-mm pitch) pinout, section 8.5
- J010 – +3.3V Power Header – 1x2 (.100 inch pitch) pinout, section 8.6

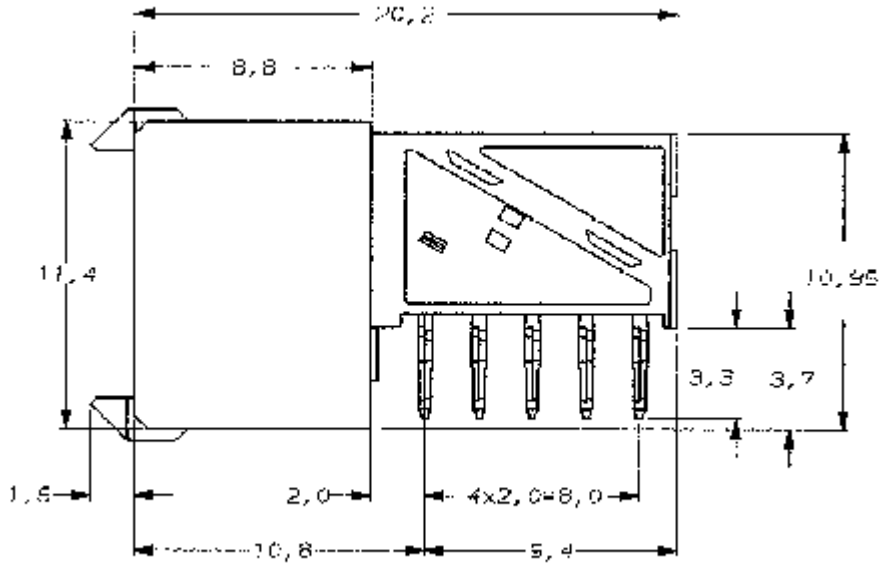
Table 5 Sample Connector Option Part Numbers

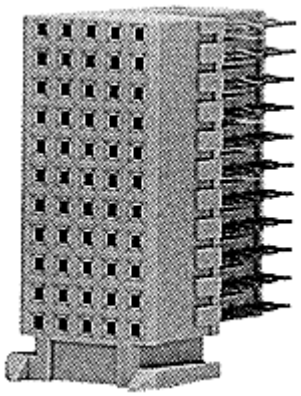
Ref	Pins	Vendor	Sample Part Number	Description
J001	64	SAMTEC SAMTEC SAMTEC	EW-32-09-G-D-xxx ESQ-132-12-G-D EW-32-09-G-D-xxx ESQ-132-14-G-D	2X32 .100 INCH NS HEADER (M) 2X32 .100 INCH NS SOCKET (F) 2X32 .100 INCH ST HEADER (M) 2X32 .100 INCH ST SOCKET (F)
J002	40	SAMTEC SAMTEC SAMTEC	EW-20-09-G-D-xxx ESQ-120-12-G-D EW-20-09-G-D-xxx ESQ-120-14-G-D	2X20 .100 INCH NS HEADER (M) 2X20 .100 INCH NS SOCKET (F) 2X20 .100 INCH ST HEADER (M) 2X20 .100 INCH ST SOCKET (F)
J003	55	AMP AMP AMP AMP	106775-1 106012-1 100159-1 100161-1	H.M. 2MM 5X11 TYPE C S-RECEPTACLE (S F) H.M. 2MM 5X11 TYPE C RA-PLUG (RA M) H.M. 2MM 5X11 TYPE C S-PLUG (S M) H.M. 2MM 5X11 TYPE C RA-RECEPTACLE (RA F)
J004	110	AMP AMP AMP AMP	352268-1 352131-1 352132-1 188836-1	H.M. 2MM 5X22 TYPE B22 S-RECEPTACLE (S F) H.M. 2MM 5X22 TYPE B22 RA-PLUG (RA M) H.M. 2MM 5X22 TYPE B22 S-PLUG (S M) H.M. 2MM 5X22 TYPE B22 RA-RECEPTACLE (RA F)
J005	10	SPECIALTY SAMTEC HARWIN	2HT05R05-4433 EW-05-09-G-D-xxx M20-998-05-08	2X5 .100 INCH R/A HEADER 2X5 .100 INCH BOARD STACKER 2X5 .100 INCH ROW POST
J007	12	MOLEX	22-05-2121	1X12 .100 INCH R/A HEADER
J008	2	MOLEX	53047-0210	1X2 1.25 MM CONNECTOR
J010	5	HARWIN	M20-999-06-06	1X5 .100 INCH ROW POST

NOTES
(1) Connectors J001,J002 are specified by the PC/104 Specification version 2.3.
(2) To interface J003,J004 to the megatel side-by-side I/O board (QTB), PC/II+dL boards are normally shipped with the two right-angle female connectors, AMP 188836-1 and AMP 100161-1 or equivalent, which mate with the two right-angle male connectors on the QTB, AMP 352131-1 and AMP 106012-1 or equivalent. The straight versions may be special-ordered. for vertical board-stacking applications, you may also order HM 2mm stacking headers.
(3) All connector part numbers are sample values; equivalent connectors may also be used.
(4) J008 mates with Molex 51021.
(5) Because a wide variety of connectors are available from a large number of sources, Megatel would be pleased to suggest mating connectors or to assist with the selection of custom connectors for your application.

6.7.1 AMP Connector (Right-Angle Receptacle) Dimensions

The following diagram and picture is representative of the AMP Z-PACK 5X11 (TYPE C) connector, one of two similar connectors used on the PC/II+dL Mass I/O Interface, and were provided by AMP. Please refer to the AMP Z-PACK HM 2MM catalog for more information.





6.8 CPLD

PC/II+dL contains a CPLD device to provide miscellaneous logic that allows the PC/II+dL to function as an AT-compatible Cpu board.

6.9 Ethernet Controller

PC/II+dL contains an optional, highly-integrated LAN Ethernet Interface, that is used in networking applications. This option includes the single-chip Crystal CS8900 controller, a configuration EEPROM, isolation transformers for either 10Base-T and/or AUI, depending upon the option ordered, and an on-board Ethernet header (J005).

PC/II+dL pulls the Attachment Unit Interface (AUI) port signals and the 10Base-T twisted-pair port signals to J005, a 10-Pin (2x5 on 0.100" [2,54-mm] spacing) header. When the Megatel Ethernet Paddle Board (an accessory board product) is attached to this header, the AUI port signals are pulled to a DB15 connector and the 10Base-T port signals are pulled to an RJ-45 connector. Alternatively, these signals can be accessed through the same connectors on standard QTB accessory transition boards which mate with the Mass I/O connector and Ethernet header.

The AUI port can be connected to an Ethernet Transceiver cable drop to provide a fully IEEE 802.3 AUI interface, while the 10Base-T interface also fully complies to IEEE 802.3.

The CS8900 controller contains an IEEE 802.3 MAC engine that operates in the I/O memory space. It contains an on-chip RAM for buffering receive & transmit frames, and supports full duplex operation, a 10BASE-T port with analog filters & automatic polarity correction, and an AUI port. Programmable transmit features include automatic re-transmission on collision, and automatic padding and CRC generation. Programmable receive features include Automatic-switch between DMA & on-chip memory, early interrupts for frame preprocessing, and automatic rejection of erroneous packets. An on-board configuration EEPROM is provided for jumper-less configuration, and on-board transformers for each interface are provided. The CS8900 supports I/O transfers at up to 10 Megabits/sec. Depending upon which media is active, the AUI or 10Base-T interface is automatically enabled. This automatic selection can be overridden by software configuration.

The CS8900 LINKLED# (Link Good LED, or Host-Controlled Output) signal drives one of the on-board LED's. This LED is, by default, configured to mark the presence of valid link pulses (Link Good). It may be reprogrammed by the customer for any other purpose, as follows:

- When the HCE0 bit of the CS8900 Self Control register (Register 15) is clear, this active-low output to the LED is low when the CS8900 detects the presence of valid link pulses;
- When the HCE0 bit is set, the host may drive this pin low by setting the HCBO in the Self Control register.

Drivers for most operating systems, including DOS, Windows and NT, are available.

For a pinout of the Ethernet header, see section 8.3.

For detailed specifications of the Ethernet Controller and Interface, see section 2.1 for datasheet titles. The document, "Ethernet Appbook", Megatel document number MT004702, also provides information on using the Ethernet feature on the PC/II+dL board.

For Ethernet order options, see section 10.3.4.

6.10 Fan Connector

The FAN connector (J008) is an option on the PC/II+dL.

For pinout information, see section 8.5.
For order information, see section 10.3.2.

For PC/II+dL systems containing a high performance version of the processor, a fan may be used for cooling purposes, depending upon the application. Lower speed processor configurations do not require a fan to be installed. However, the thermal characteristics of the enclosure may dictate the use of a fan, and this depends upon the application.

A fan connector is can be ordered by option. This connector is a 1X2 1.25-mm MOLEX 53047-0210 type connector, or equivalent as required by the user. Other 1X2 1.25-mm headers of connectors can be CUSTOM specified by the user.

6.11 Flash ROM – BIOS

The standard ROM on the PC/II+dL is a 2Mbit (256 KB) flash EEPROM. This EEPROM contains the system BIOS and all option BIOS modules, including the SVGA BIOS, the SCSI BIOS and other bios modules required to interface to on-board peripherals. All PC/II+dL boards are shipped with a flash BIOS.

BIOS code is shadowed in system memory located between 0x000C0000 and 0x000FFFFF. The system BIOS code occupies the top segment of real mode memory (0x000F0000 to 0x000FFFFF). Option ROM BIOS modules are shadowed into the region 0x000C0000 to 0x000DFFFF. Option BIOS modules will be loaded depending upon the configuration of the PC/II+dL board.

For a particular customization of the BIOS or its parameters, please contact Megatel engineering.

The following tables describe the drivers that are available for use with the PC/II+dL board. Both drivers and optional ROM BIOS modules are listed. Please contact Megatel if you have specific requirements, and to receive the driver information, or visit our web site.

Table 6 ETHERNET Drivers & Utilities

Driver Name	Revision
Netware ODI DOS Client	2.62
Netware ODI OS/2 Client	2.59
Netware ODI Server Driver	2.60
OS/2 NDIS2 Driver	2.68
DOS NDIS2 Driver	2.68
Windows NT/95 NDIS3 Driver	3.20
Windows for Workgroup NDIS3 Driver	2.57
Packet Driver	2.55
Setup utility	2.66

Table 7 VIDEO Drivers & BIOS Options

Driver Name	Revision
HiQVideo Driver for Win NT 3.5x	1.1.5
HiQVideo Driver for Win 95	1.2.6
Display Driver for Windows 3.x	1.3.2
Display Driver for OS/2	2.2.7
HiQVideo VGA BIOS	2.0.0

Table 8 FLASH Array BIOS Option

Driver Name	Revision
Datalight CardTrick (as Optional ROM)	3.01.13

6.12 Flash Array – User

PC/II+dL contains an optional 2 MB, 4 MB or 8 MB of Flash Array. PC/II+dL uses Intel® StrataFlash™ or FlashFile™ high-density symmetrically-blocked architecture flash memory. Flash Array parts are soldered on the circuit board. The flash array is supported by the Datalight Cardtrick BIOS driver.

All required programming voltages are provided on-board.

For Flash Array order options, see section 10.3.6.

6.13 Flash Disk – M-Systems Disk-on-Chip

PC/II+dL contains an optional 32-Pin DIP socket that can be user-populated with a Solid-State Disk such as M-Systems Disk-on-Chip® 2000 flash disk. The Flash Disk Socket option provides the ob-board socket which is bottom-mounted on the PC/II+dL circuit board, to be populated by the user.

The Disk-on-Chip® product provides standalone or expansion Flash Disk memory in sizes ranging up to 288 MB or greater.

Both the DiskOnChip® 2000 and Flash Array can be used together on the same board.

For more detailed information on Disk-on-Chip® products, please contact M-Systems or visit their web site.

For information on the Flash Disk Socket order option, see section 10.3.7.

6.14 Floppy Disk Interface

PC/II+dL contains an integrated Floppy Disk Drive Interface controller that is provided by the ACC Micro ACC 2089. The Floppy interface is always present on the board, and Floppy disk interface signals are pulled to the Mass I/O Connector.

The controller supports one (1) or two (2) 3.5" floppy disk drives. It is compatible with IBM System 34 double density format (MFM), and Sony EMCA format. Address decoding is compatible with the IBM PC drive system. Both DMA and non-DMA modes are supported. Standard 500, 250 and 300 Kb/Sec transfer rates are supported.

The Floppy Disk controller uses Interrupt Request IRQ6, and DMA channel DRQ2.

The floppy disk interface can be multiplexed to the parallel port pins for external floppy disk drive support. This function is enabled by setting Register BEh, Bit 2, to one.

For more information about the Floppy Disk Interface, please refer to the ACC 2089 datasheet, found in section 2.1 of this document.

For Mass I/O order information, see sections 10.3.18 and 10.3.19.
For Floppy I/O Interface pinout information, see section 8.2.7.

6.15 Keyboard & Mouse

PC/II+dL contains an integrated AT-style Keyboard & PS/2-style Mouse controller. The keyboard is always present, requiring only the Mass I/O 5X22 (J004) connector. The Mouse is optional, and when ordered, it also requires the Mass I/O 5X22 (J004) connector to be ordered.

For pinout information, see sections 8.2.9 and 8.2.10.
For order information for the Mouse, see section 10.3.12.
For order information for the Mass I/O 5X22 (J004) connector, see section 10.3.19.
For more detailed information about the keyboard & mouse, please refer to the PC97338 and ACC 2089 datasheets, found in section 2.1.

6.16 Memory

The PC/II+dL board has been manufactured to contain one to 4 parts of soldered-down EDO DRAM-type memory. EDO DRAM devices are normally EDO 60 ns parts, and the total installed memory is an order option.

There are 4 population sites on the board for the two banks of soldered-down EDO DRAM. Either 1Mx16 or 4Mx16 parts are installed. The options are as follows:

Table 9 EDO DRAM Memory Options

Total Memory	Devices x Organization
4 MB	2 x 1Mx16
8 MB	4 x 1Mx16
16 MB	2 x 4Mx16
32 MB	4 x 4Mx16

For information on the Memory order options, see section 10.3.10.

6.17 Mouse

Refer to section 6.15, Keyboard & Mouse.

6.18 Parallel Port

PC/II+dL supports a single Parallel Port controller that is integrated in the ACC 2089 super I/O. The parallel port is a basic feature of PC/II+dL, and requires only the Mass I/O 5X22 (J004) connector to be installed.

The parallel port interface supports a standard selectable ECP/EPP/BPP/SPP mode. The parallel port supports standard Centronics-type printers, standard PS/2-type Bi-directional devices, and Enhanced Parallel Port (EPP 1.9) and Extended Capabilities Port (ECP) protocols. A 16-byte FIFO is included in the interface, used by EPP and ECP modes. Run-Length Compression (RLE) is also supported. Both DMA and PIO transfers are supported.

The parallel port is software configurable – there are no jumpers required.

For pinout and signal information for the Parallel Port, see section 8.2.13.
For detailed parallel port specifications, please refer to the datasheets for the ACC 2089, section 2.1.

6.19 PC/104 Bus Interface

The PC/II+dL board complies to the PC/104 specification in physical form factor and electrical interface. The board is stackable, usually at the top of the stack, using stacking type PC/104 connectors that are mounted on the PC/II+dL board.

Please refer to the documents, "PC/104 specification – Revision 2.3 – June 1996" and "P996.1 Standard or Compact Embedded-PC Modules", listed in section 2.2.

For Bus Drive Current requirements, refer to section 5.5.
For pinout information for the PC/104 connector, see section 8.1.
For order information about the PC/104 connectors, see section 10.3.17.
For part number information, refer to section 6.7.

6.20 Real-Time Clock

The PC/II+dL contains an optional Real-Time Clock (RTC), a Dallas Semiconductor DS1685. This clock is a full-function part, and is certified as Year-2000 compliant by Dallas. The RTC uses a 32.768 KHz crystal and a 3.0V Lithium battery. The battery is soldered onto the circuit board and is part of the RTC option.

Information contained in the following sub-sections is present in summary form.

For detailed information about the Real-Time Clock, see the DS1685 datasheet found in section 2.1.
For Real-Time clock order option information, see section 10.3.14.
For information on how the RTC's Lithium Battery affects characterization of the board, see section 5.1 Note 3, and section 5.2 Note 1.

6.20.1 Features of the Real-Time Clock

- 242 Bytes battery backed up NVRAM
- RAM Clear input
- Low battery current (500 nA)
- Leap Year to year 2100 provides Y2K compliance
- Century byte with Automatic Rollover provides Year 2000 compliance
- 24 0r 12 Hour Format
- Programmable Alarm, Settable at Any Time hh:mm:ss, with Interrupt
- Programmable Timer, Settable to Periods Ranging from 122 uSec to 500 mSec
- Daylight Savings Time Support
- Unique 48-Bit Silicon Laser-Written Serial Number, Can be used by Customer Applications

The PC/II+dL is factory-shipped with the Real-Time Clock set to the correct time and date for the North-American EST (Eastern Standard Time) time zone. The software for the Real-Time Clock is included in the system BIOS for boards containing the Real-Time Clock option.

6.20.2 Lithium Battery

The Lithium battery is rated for 125 mAh (typical) in an operating range of -20C to +70C. Discharge current is 500 nA, and storage temperature is -40C to +60C.

Warning: Lithium batteries require special handling, always follow the manufacturer's handling instructions, and never exceed the ratings given by the manufacturer or provided in this document.

6.20.3 Setting Time and Date

The DOS clock is updated automatically by the Real-Time Clock upon Boot-Up. Should you change the time or date in DOS, the PC/II+dL will conversely update the Real-Time Clock hardware time and date. The PC/II+dL uses standard DOS instructions to change the time and date. If you are using standard DOS, and if the time and date are displayed at boot time, you may at that point change the time and date if desired. Standard DOS commands to change the TIME and DATE can also be used.

Time and date are also settable in Windows and Windows NT4.0; please refer to the operating system documentation for details.

6.20.4 Using the Real-Time Clock NVRAM

The BIOS utilizes the battery backed up NVRAM to store its configuration information which it needs to access at boot time and at other times. Besides the time and data information contained in the Real-Time Clock hardware, the BIOS stores information about the Video preferences, floppy disk drive configuration, and panel information.

A total of 114 Bytes of RAM in bank 0, and 128 Bytes of RAM in bank 1 are supported (total of 242 Bytes of RAM).

6.20.5 Real-Time Clock Interrupt 1Ah

The BIOS supports AT compatible real-time clock functions using software interrupt 1Ah. In addition, the PC/II+dL BIOS supports the following functions using the software interrupt 1Ah, which provide read and write access to bank 0 and bank 1 SRAM memory in the real-time clock, and read access to the unique serial number encoded in the real-time clock chip.

1. FUNCTION 0FFh – WRITE AND READ BANK-0 SRAM

This function writes a byte to RTC SRAM Bank 0, or reads a byte from RTC SRAM Bank 0.

```
MOV    AH,0FFh
MOV    DL,<RTC bank 0 register number>
MOV    DH,<Direction>                  Bit 0 = 0 (WRITE), Bit 0 = 1 (READ)
                                       Bit 1-7 = Unused
MOV    AL,<8-Bit Value to be Written>  Used if DH.0 = 0, Unused if DH.0 = 1
INT    1Ah
-- returns here with
       /FX.CF = 1 (Error)
       /FX.CF = 0 (No Error)
              /AH = Destroyed
              /AL = value read from RTC or written to RTC>
```

2. FUNCTION 0FBh – WRITE AND READ BANK-1 EXTENDED SRAM

This function writes a byte to RTC Bank 1 Extended SRAM, or reads a byte from RTC Bank 1 Extended SRAM.

```
MOV    AH,0FBh
MOV    DL,<RTC bank 1 register number>  0 – 7Fh
MOV    DH,<Direction>                   Bit 0 = 0 (WRITE), Bit 0 = 1 (READ)
                                        Bit 1-7 = Unused
MOV    AL,<8-Bit Value to be Written>   Used if DH.0 = 0, Unused if DH.0 = 1
INT    1Ah
-- returns here with
       /FX.CF = 1 (Error)
       /FX.CF = 0 (No Error)
              /AH = Destroyed
              /AL = value read from RTC or written to RTC>
```


3. FUNCTION 0FCh – READ RTC SERIAL NUMBER

This functions reads the silicon serial number that is embedded in the RTC chip. Each RTC chip is manufactured to contain a unique serial number.

```
MOV     AH,0FCh
LES     DI,<pointer to seven-byte buffer that will receive the serial number field>
INT     1Ah
-- returns here with
        /FX.CF = 1 (Error)
        /FX.CF = 0 (No Error)
                /[ES:DI+0] = Silicon Serial Number Byte 1 through Byte 6
                /[ES;DI+6] = Silicon Serial Number CRC byte
```


6.20.6 Real-Time Clock Memory Map

Table 10 Real-Time Clock Memory Map

RTC	Bank 0		Bank 1	
Offset	Description	Access	Description	Access
00	Seconds	R(bits 0-7),W(bits 0-6)	Seconds	R(bits 0-7),W(bits 0-6)
01	Seconds Alarm	RW	Seconds Alarm	RW
02	Minutes	RW	Minutes	RW
03	Minutes Alarm	RW	Minutes Alarm	RW
04	Hours	RW	Hours	RW
05	Hours Alarm	RW	Hours Alarm	RW
06	Day of the Week	RW	Day of the Week	RW
07	Day of the Month	RW	Day of the Month	RW
08	Month	RW	Month	RW
09	Year	RW	Year	RW
0A	Register A	R(bits 0-7), W(bits 0-6)	Register A	R(bits 0-7), W(bits 0-6)
0B	Register B	RW	Register B	RW
0C	Register C	R	Register C	R
0D	Register D	R	Register D	R
0E-3F	RAM Bytes 00-3F		RAM Bytes 00-3F	
40	RAM Byte 40		RTC Model Number	
41	RAM Byte 41		1st Byte Serial Number	
42	RAM Byte 42		2nd Byte Serial Number	
43	RAM Byte 43		3rd Byte Serial Number	
44	RAM Byte 44		4th Byte Serial Number	
45	RAM Byte 45		5th Byte Serial Number	
46	RAM Byte 46		6th Byte Serial Number	
47	RAM Byte 47		CRC Byte	
48	RAM Byte 48		Century Byte	
49	RAM Byte 49		Date Alarm	
4A	RAM Byte 4A		Extended Control Reg 4A	
4B	RAM Byte 4B		Extended Control Reg 4B	
4C	RAM Byte 4C		Reserved	
4D	RAM Byte 4D		Reserved	
4E	RAM Byte 4E		RTC Address – 2	
4F	RAM Byte 4F		RTC Address – 3	
50	RAM Byte 50		Extended RAM Address	
51	RAM Byte 51		Reserved	
52	RAM Byte 52		Reserved	
53	RAM Byte 53		Extended RAM Data Port	
54-7F	RAM Bytes 54-7F		Reserved	

Table 11 RTC Extended RAM Memory Map

Via 50 & 53	Bank 0		Bank 1 Extended RAM	
00-7F	-		RAM Bytes 00-7F	RW

6.21 Reset Switch

PC/II+dL responds to a "reset switch" signal input (MR-RSTSW#) from the Mass I/O Connector (J004, pin e8). The reset switch signal is Active Low. It should be left unconnected if unused. See SIGNAL DESCRIPTION in section 8.2.11 for requirements.

The on-board supervisor asserts System RESET for as long as MR-RSTSW# is held low, and for 130 to 200 ms after this signal is floated. An on-board pull-up of 40 KΩ is used.

For pinout information and requirements, see section 8.2.11.
For information on ordering the Mass I/O 5X22 (J004) connector, see section 10.3.19.

6.22 SCSI I/O

PC/II+dL contains an optional SCSI controller. The SCSI bus signals are pulled to the Mass I/O Connector. Active terminators, with a jumper to enable or disable the terminators, is available using a Megatel standard QTB (transition board which provides connectors to interface to all standard devices).

The SCSI interface uses Interrupt Request IRQ11.
The SCSI interface uses DMA channel DRQ6.

For pinout and signal information, see section 8.2.14.
For information on ordering the SCSI option, see section 10.3.9.

Adaptec AIC6360 Controller

When ordered, the Adaptec AIC-6360 SCSI-2 controller is used as the Host device on a SCSI-2 bus. This controller supports byte, word or 32-bit double word PIO data transfers, and can also utilize 16-bit DMA. With its 128-byte data FIFO, it can burst data at up to 10 MBytes/s across the Host bus, and can support synchronous data transfers at up to 10 MBytes/sec across the SCSI bus.

PC/II+dL BIOS ships with a SCSI option BIOS module. In addition, an installable Adaptec driver (ASPI manager for DOS) is available which supports a range of devices and operating environments. For more details, please refer to the Adaptec SCSI documentation, available from Adaptec.

6.23 Serial Ports

PC/II+dL contains 1, 2, 3 or 4 optional full RS-232E ports.

For pinout and signal information, see section 8.2.3.
For information on Serial Port order codes, see section 10.3.13.
For more detailed information about serial I/O, please refer to the PC97338 and ACC 2089 datasheets, found in section 2.1.

Each serial port option includes all required RS-232 receivers and line drivers.
Each serial port is fully 16C550 compatible.
Each serial port contains standard modem control and data I/O interface signals (2-data, 6-control).
Each serial port contains both receive and transmit FIFOs which are 16-bytes deep.

PC/II+dL uses the ADM211E receiver/driver on each serial interface to provide RS-232 levels. The transceiver is EIA-RS232E and CCITT V.28 compliant. Input tolerance on all inputs is ±25V, and output swing on all outputs is ±9V with all transmitter outputs loaded with 3K ohms to Ground. The transceivers run at +5V and use on-chip voltage doublers and inverters. Refer to the ADM211E datasheet for determining the power which may be drawn by attached devices.

The I/O ports are configured by the BIOS as COM1, COM2, COM3 and COM4.

COM1 uses Interrupt Request IRQ4, and is based in I/O address space at 3F8h.
COM2 uses Interrupt Request IRQ3, and is based in I/O address space at 2F8h.
COM3 uses Interrupt Request IRQ4, and is based in I/O address space at 3E8h.
COM4 uses Interrupt Request IRQ3, and is based in I/O address space at 2E8h.

6.24 Speaker Output

Output sound waveform signals carried by the Speaker Output signal are generated by Timer 2. The Timer 2 output is gated with port 60h, bit 1 (Speaker Data) to drive the Speaker Output. The state of Timer 2 output can be read from port 61h, bit 5.

Speaker Output signal is pulled to the Mass I/O Connector (MS-SPEAKER, pin J004-a7 on 5X22 Mass I/O Connector). It is intended to drive a piezo-electric audio transducer connected between the Speaker Output signal pin and Ground. The Speaker Output logic is always part of the PC/II+dL board; the Mass I/O connector is an option and is required to use the PC Speaker.

For information on the Mass I/O connector, see section 8.2.

For pinout & signal information for the PC Speaker, see section 8.2.12.
For information on the Mass I/O order option, see sections 10.3.18 and 10.3.19.

6.25 Super AT I/O Controllers

AT Super-I/O functionality is provided by two controllers. The ACC MICRO 2089 is part of the basic board functionality while the National PC97338 is an optional controller that is populated when Serial ports COM3 and COM4 are present.

Both controllers provide the 4 full 16550-style UARTs with 16-byte FIFOs (full on-board RS232 transceivers are supported), a Parallel ECP/EPP port (also configurable as BPP/SPP), a PS/2-style Keyboard and PS/2 Mouse, an IDE controller with support for two devices, and a standard Floppy controller with support for two 3.5” drives. Additional standard features include generation of PC speaker output, and system reset switch input.

The functionality provided by the two controllers are described in their respective sections in this document.

For more detailed information about these controllers, please refer to the PC97338 and ACC 2089 datasheets, found in section 2.1.

6.26 Timers/Counters

Three internal counters are provided as basic features of PC/II+dL. The timers/counters are compatible to the AT standard 8254. The clock input for each is tied to a clock of 1.193 MHz, which is derived by dividing the system 14.31818 MHz clock by 12, and which provides a minimum timing resolution of 838 ns.

Timer 0 output is tied to IRQ0 (Interrupt controller 1, level 0).
Timer 1 output is used to initiate a refresh cycle for system memory.
Timer 2 is used to generate signals that produce sound waveforms on the Speaker Output signal.

6.27 Video – CT 65550 Super VGA & Panel Controller

PC/II+dL contains a complete analog and flat panel Video interface. When this optional interface is shipped on a PC/II+dL board, the analog CRT display and 24-bit flat panel interface signals are pulled to the Mass I/O connector. The Video Interface option includes 2 MB of fast video memory EDO DRAM.

The Video Interface uses the Chips® 65550 Video Controller and is compatible with the IBM-PS/2 Video Graphics Array (VGA) and supports the SVGA standard. The controller operates on the local bus, and supports both Analog Monitors and a wide variety of Flat Panels. It contains a powerful 64-bit Graphics Engine, Palette/DAC and Clock Synthesizer. The separate 2 MB of fast EDO DRAM video memory is accessed from the controller over a direct 32-Bit bus. This video memory is used normally, to buffer all video data and is mapped by the controller into Main memory address space. It is also used for frame buffering in LCD-DD interfaces – unused video memory is automatically used for a framestore area by the controller in this case. The hardware register and gate interface is standard VGA, and the BIOS is also VGA compatible. Drivers for all common operating systems are available. Simultaneous CRT and LCD display mode is available.

The Video panel interface can be ordered to support either 5V panels or 3.3V panels. This option affects both the 24-bit panel interface and the compatible video interface. For more information on using the 3.3V panel interface, contact Megatel Engineering.

For pinout and signal information, see sections 8.2.15 (CRTs) and 8.2.8 (Panels).
For order information for the video feature, see section 6.27.
For order information for the panel ENAVEE polarity option, see section 10.3.4.
For information on the Video Hardware, see section 6.27.1.
For information on the Chips Video driver and BIOS, see sections 6.27.2 and 6.27.3.
For information on Video Display enhancement features of the 65550 controller, see section 6.27.4.
For information on the use of the Linear Video buffer, see section 6.27.5.
For information on Video CRT support, see section 6.27.6.
For information about Panel support, see section 6.27.7.
For information about Modes and Resolutions supported, see sections 6.27.8, 6.27.9 and 6.27.10.

6.27.1 Video Hardware Features

Please refer to the Intel/Chips® 65550 reference documentation for a list of features available. The 65550 supports these features (revision 1.5):

- Highly integrated design Flat Panel and CRT GUI Accelerator & Multimedia Engine, Palette/DAC, and Clock Synthesizer
- Hardware Windows Acceleration
  - 64-bit Graphics Engine
    - System-to-Screen and Screen-to-Screen BitBLT
    - 3-Operand Raster-Ops
    - 8/16/24 Color Expansion
  - Transparent BLT
    - Optimized for Windows™ BitBLT format
- High Performance:
  - Deep write buffers
  - EDO DRAM Support
  - 40 MHz
- Display centering and stretching features for optimal fit of VGA graphics and text on 800x600 and 1024x768 panels
- Simultaneous Hardware Cursor and Pop-up Window
  - 64x64 pixels by 4 colors
  - 128x128 pixels by 2 colors
- Game Acceleration
  - Source Transparent BLT
  - Destination Transparent BLT

  - Double buffer support for YUV and 15/16bpp Overlay Engine
  - Instant Full Screen Page Flip
  - Read back of CRT Scan line counters.
- Optimized for High-Performance Flat Panel Display
  - 640x480 x 24bpp
  - 800x600 x 24bpp
  - 1024x768 x 16bpp

  CRT Support 110 MHz
- Direct interface to Color and Monochrome, Single Drive (SS), and Dual Drive (DD), STN & TFT panels
- Flexible On-chip Activity Timer facilitates ordered shut-down of the display system
- Composite NTSC / PAL Support
- Power Sequencing control outputs regulate application of Bias voltage
- Fully Compatible with IBM® VGA

6.27.2 Video Driver Features

- High Performance Accelerated drivers
- Compatible across HiQVideo family
- Auto Panning Support
- LCD/CRT/Simultaneous Mode Support
- Auto Resolution Change
- HW Stretching/Scaling
- Double Buffering
- Internationalization
- ChipsCPL (Control Panel Applet)
- Direct Draw support
- Games SDK support
- Dynamic Resolution Switching
- VGA Graphics applications in Window
- VESA DDC extensions
- VESA DPMS extensions
- Property Sheet to change Refresh/Display
- Seamless Windows Support
- Boot time resolution adjustment
- DIVE, EnDIVE
- DCAF
- DebugVGA
- Auto testing of all video modes
- ChipsVGA
- ChipsEXT
- BIOS OEM Reference Guide
- Display Driver User's Guide
- Utilities User's Guide
- Release Notes for BIOS, Drivers, and Utilities

6.27.3 Video BIOS Features

- VGA Compatible BIOS
- DDC 1, DDC 2AB
- Text and Graphics Expansion
- Auto Centering
- 44 (40) K BIOS
- CRT, LCD, Simultaneous display modes
- Auto Resolution Switch

- Multiple Refresh Rates
- NTSC/PAL support
- Extended Modes
- Extended BIOS Functions
- 1024x768 TFT, DSTN Color Panels
- Multiple Panel Support (8 panels built in)
- Get Panel Type Function
- HW Popup Interface
- Monitor Detect
- Pop Up Support
- SMI and Hot Key support
- Set Active Display Type Hook
- Save/Restore Video State Hook
- Setup Memory for Save/Restore Hook
- SMI Entry Point Hook
- Int 15 Calls after POST, Set Mode Hook

6.27.4 Video Display Enhancement Features

A variety of video enhancement features are supported, particularly for flat panels, by the Chips® 65550 Video Controller:

True-Gray

PC/II+dL video supports TRUE-GRAY gray scale algorithm, a polynomial-based frame-rate control (FRC) and dithering algorithm to generate a maximum of 61 gray levels on monochrome panels. This algorithm extends the support of flicker-free gray scales from 16 to 61 on, for example, film-compensated monochrome STN LCDs, without the need to increase refresh rate, a conventional solution which increases power consumption, ghosting and decreases contrast.

RGB Color to Gray Scale Reduction

PC/II+dL video supports RGB Color to Gray Scale Reduction, allowing 24-bit color pallette data to be reduced automatically to 6-bits for 64 gray scales. Reduction techniques include NTSC weighting, Equal Weighting (for blue background operating systems such as Windows), and Green Only for replicating 6-bits of green pallette data such as IBM monochrome monitors.

SmartMap

PC/II+dL video supports SMARTMAP, an algorithm that automatically adjusts the foreground and background of adjacent gray scales to maximize contrast on flat panel displays. This algorithm is particularly useful when displaying information containing multiple colors on monochrome flat panels.

Text Enhancement

PC/II+dL video supports Text Enhancement whereby Dim White is displayed on flat panels as Bright White to optimize contrast level.

Vertical Compensation

PC/II+dL video supports Vertical Compensation techniques for flat panels. Unlike CRT monitors, flat panels have a fixed number of scan lines (eg. 200, 400, 480 or 768 lines). PC/II+dL allows lower resolution software to be displayed on a higher resolution panel by use of manual or automatic Vertical Centering, Stretching, Blank Line Insertion, or Tall Font™.

Horizontal Compensation

PC/II+dL video supports Horizontal Compensation techniques for flat panels, including Horizontal Compression, Horizontal Centering and Horizontal Doubling and text expansion.

6.27.5 Video Linear Buffer Support

PC/II+dL video frame buffer is supported using 2 MB of fast EDO DRAM. This memory can be mapped by the 65550 controller (under program control by the Video BIOS) (a) at the standard VGA memory window (0x000A0000 through 0x000BFFFF), or (b) into a linearly-accessible 8 MB memory window at an origin located above the system's main memory address space. The video driver will use linear mode if it is available because performance is enhanced in that case.

The 65550 controller normally requires the use of the two pins, ACTI and ENABKL which are normally used for Panel support, for mapping DRAM at or above the 64 MB boundary. For the PC/II+dL, this linear buffer will normally be mapped at the 32 MB boundary, and therefore ACTI and ENABKL are always available for normal Panel usage. If required, the ACTI+ENABKL option should therefore always be ordered using code "0".

6.27.6 Video Analog CRT Display Support

PC/II+dL supports high resolution fixed frequency and variable frequency analog monitors in interlaced and non-interlaced modes of operation. The video controller supports up to 110 MHz, which provides SVGA resolutions up to 1280 x 1024 – 256 colors, 1024 x 768 – 256K colors or 800 x 600 – 1,677,216 colors. Please refer to the Chips® 65550 documentation for detailed information, see section 2.1.

All standard VGA modes are supported on these typical CRT monitors: PS/2 fixed frequency analog CRT monitor or equivalent (31.5 / 33.5 KHz horizontal frequency specification); NEC Multi-Sync 3D or equivalent multi-frequency CRT monitor (37.5 KHz minimum horizontal frequency specification); Nanao Flexscan 9070s, Multisync 5D, or equivalent multi-frequency high-performance CRT monitor (48.5 KHz minimum horizontal frequency specification).

6.27.7 Video Flat Panel Display Support

The on-board Chips 65550 controller supports all flat panel display technologies, including plasma, electro-luminescent (EL) and liquid crystal (LCD). LCD panel interfaces are provided for single panel, single drive (SS) and dual panel, dual drive (DD) configurations. The controller utilizes the on-board video memory for its integrated frame buffer and 24-bit panel interface; the "C" DRAM is not used on the PC/II+dL. Standard and high-res passive STN and active matrix TFT/MIN LCDs are supported. Up to 16M colors on 24-bit active matrix LCDs, up to 4K colors on passive STN LCDs and up to 64 gray scales on monochrome panels are supported. The flat panel interface can interface to a variety of panels, as illustrated in the following table; please refer to the Chips® 65550 Video Controller reference documentation for details.

Table 12 Flat Panel Interface Signal Mapping

Mass I/O J004		65550		Panel Interface (by Type of Panel)										
Pin Name	Pin #	Pin Name	Pin #	Mono SS 8-bit	Mono DD 8-bit	Mono DD 16-bit	Color TFT 9/12/ 16 bit	Color TFT 18/24 bit	Color TFT HR 18/24 bit	Color STN SS 8-bit (x4bP)	Color STN SS 16-bit (4bP)	Color STN DD 8-bit (4bP)	Color STN DD 16-bit (4bP)	Color STN DD 24-bit
L1-FPD0	e6	P0	71	–	UD3	UD7	B0	B0	B00	R1	R1	UR1	UR0	UR0
L1-FPD1	a5	P1	72	–	UD2	UD6	B1	B1	B01	B1	G1	UG1	UG0	UG0
L1-FPD2	b5	P2	73	–	UD1	UD5	B2	B2	B02	G2	B1	UB1	UB0	UB0
L1-FPD3	c5	P3	74	–	UD0	UD4	B3	B3	B03	R3	R2	UR2	UR1	LR0
L1-FPD4	d5	P4	75	–	LD3	UD3	B4	B4	B10	B3	G2	LR1	LR0	LG0
L1-FPD5	e5	P5	76	–	LD2	UD2	G0	B5	B11	G4	B2	LG1	LG0	LB0
L1-FPD6	a4	P6	78	–	LD1	UD1	G1	B6	B12	R5	R3	LB1	LB0	UR1
L1-FPD7	b4	P7	79	–	LD0	UD0	G2	B7	B13	B5	G3	LR2	LR1	UG1
L1-FPD8	c4	P8	81	P0	–	LD7	G3	G0	G00	SHFCLKU	B3	–	UG1	UB1
L1-FPD9	d4	P9	82	P1	–	LD6	G4	G1	G01	–	R4	–	UB1	LR1
L1-FPD10	e4	P10	83	P2	–	LD5	G5	G2	G02	–	G4	–	UR2	LG1
L1-FPD11	a3	P11	84	P3	–	LD4	R0	G3	G03	–	B4	–	UG2	LB1
L1-FPD12	b3	P12	85	P4	–	LD3	R1	G4	G10	–	R5	–	LG1	UR2
L1-FPD13	c3	P13	86	P5	–	LD2	R2	G5	G11	–	G5	–	LB1	UG2
L1-FPD14	d3	P14	87	P6	–	LD1	R3	G6	G12	–	B5	–	LR2	UB2
L1-FPD15	e3	P15	88	P7	–	LD0	R4	G7	G13	–	R6	–	LG2	LR2
L1-FPD16	a2	P16	90	–	–	–	–	R0	R00	–	–	–	–	LG2
L1-FPD17	b2	P17	91	–	–	–	–	R1	R01	–	–	–	–	LB2
L1-FPD18	c2	P18	92	–	–	–	–	R2	R02	–	–	–	–	UR3
L1-FPD19	d2	P19	93	–	–	–	–	R3	R03	–	–	–	–	UG3
L1-FPD20	e2	P20	94	–	–	–	–	R4	R10	–	–	–	–	UB3
L1-FPD21	b1	P21	95	–	–	–	–	R5	R11	–	–	–	–	LR3
L1-FPD22	d1	P22	96	–	–	–	–	R6	R12	–	–	–	–	LG3
L1-FPD23	e1	P23	97	–	–	–	–	R7	R13	–	–	–	–	LB3
L1-SHFCLK	d6	SHFCLK	70	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK
Pixels/Clock				8	8	16	1	1	2	2-2/3	5-1/3	2-2/3	5-1/3	8

NOTES:
(1) The 65550 also supports panel interfaces that transfer one pixel per word, but which use both edges of SHFCLK to transfer one pixel on each edge.
(2) The higher order output lines should be used when only 9 or 12 bits are needed from the 9/12/16-bit TFT interface, or when only 18 bits are needed from the 18/24-bit TFT or TFT HR interfaces. The lower order bits should be left unconnected.

6.27.8 Video Mode Support – Standard VGA Modes

Which super VGA Graphics modes the Chips® 65550 can support depend upon several factors, including display memory size requirements, dot clock (display pixel rate) requirements, video DRAM memory bandwidth requirement (bytes per pixel, pixel rate and bandwidth available to the CPU). For simultaneous CRT and panel operation, compatibility between panel timing requirements and CRT requirements is also a factor. The PC/II+dL Chips® 65550 uses a 32-bit interface to 2 MB of 50 ns (typical) EDO DRAM memory. It runs at 5V and supports a maximum Dot Clock (DCLK) of 110 MHz. The standard VGA modes supported by the PC/II+dL are summarized in the following table.

Table 13 VGA Standard Modes Supported

Mode# (Hex)	Display Mode	Colors	Text Display	Font Size	Pixel Resolution	DotClock (MHz)	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
0, 1	Text	16	40 x 25	8x8	320x200	25.175	31.5	70
0*,1*	Text	16	40 x 25	8x14	320x350	25.175	31.5	70
0+,1+	Text	16	40 x 25	9x16	360x400	28.322	31.5	70
2,3	Text	16	80 x 25	8x8	640x200	25.175	31.5	70
2*,3*	Text	16	80 x 25	8x14	640x350	25.175	31.5	70
2+,3+	Text	16	80 x 25	9x16	720x400	28.322	31.5	70
4	Graphics	4	40 x 25	8x8	320x200	25.175	31.5	70
5	Graphics	4	40 x 25	8x8	320x200	25.175	31.5	70
6	Graphics	2	80 x 25	8x8	640x200	25.175	31.5	70
7	Text	Mono	80 x 25	9x14	720x350	25.175	31.5	70
7+	Text	Mono	80 x 25	9x16	720x400	28.322	31.5	70
D	Planar	16	40 x 25	8x8	320x200	25.175	31.5	70
D	Planar	16	80 x 25	8x8	640x200	25.175	31.5	70
F	Planar	Mono	80 x 25	8x14	640x350	25.175	31.5	70
10	Planar	16	80 x 25	8x14	640x350	25.175	31.5	70
11	Planar	2	80 x 30	8x16	640x480	25.175	31.5	60
12	Planar	16	80 x 30	8x16	640x480	25.175	31.5	60
13	Packed Pixel	256	40 x 25	8x8	320x200	25.175	31.5	70

NOTES:
(1) All of the above VGA standard modes are supported directly in the Video BIOS.
(2) All VGA modes using 25.175 MHz and 28.322 MHz can also be supported using 32 MHz and 36 MHz respectively.

Table 14 Extended Resolution Modes Supported – Preliminary

Mode# (Hex)	Display Mode	Colors	Text Display	Font Size	Pixel Resolution	DotClock (MHz)	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
20	4-bit Linear	16	80x30	8x16	640x480	25.175	31.5	60
20	4-bit Linear	16	80x30	8x16	640x480	31.500	37.9	72
20	4-bit Linear	16	80x30	8x16	640x480	31.500	37.5	75
22	4-bit Linear	16	100x37	8x16	800x600	36.000	35.1	56
22	4-bit Linear	16	100x37	8x16	800x600	40.000	37.9	60
22	4-bit Linear	16	100x37	8x16	800x600	50.350	48.1	72
22	4-bit Linear	16	100x37	8x16	800x600	49.500	46.9	75
24 I	4-bit Linear	16	128x48	8x16	1024x768	44.900	35.5	43
24	4-bit Linear	16	128x48	8x16	1024x768	65.000	48.4	60
24	4-bit Linear	16	128x48	8x16	1024x768	75.575	57.5	70
24	4-bit Linear	16	128x48	8x16	1024x768	78.750	60	75
28 I	4-bit Linear	16	128x48	8x16	1280x1024	78.750	46.433	43
28	4-bit Linear	16	128x48	8x16	1280x1024	80.000	80.0	43
30	8-bit Linear	256	80x30	8x16	640x480	25.175	31.5	60
30	8-bit Linear	256	80x30	8x16	640x480	31.500	37.9	72
30	8-bit Linear	256	80x30	8x16	640x480	31.500	37.5	75
32	8-bit Linear	256	100x37	8x16	800x600	36.000	35.1	56
32	8-bit Linear	256	100x37	8x16	800x600	40.000	37.9	60
32	8-bit Linear	256	100x37	8x16	800x600	50.350	48.1	72
32	8-bit Linear	256	100x37	8x16	800x600	49.500	46.9	75
34 I	8-bit Linear	256	128x48	8x16	1024x768	44.900	35.5	43
34	8-bit Linear	256	128x48	8x16	1024x768	65.000	48.4	60
34	8-bit Linear	256	128x48	8x16	1024x768	75.575	57.5	70
34	8-bit Linear	256	128x48	8x16	1024x768	78.750	60.00	75
40	15-bit Linear	32K	80x30	8x16	640x480	50.350	31.5	60
40	15-bit Linear	32K	80x30	8x16	640x480	63.000	37.9	72
40	15-bit Linear	32K	80x30	8x16	640x480	63.000	37.5	75
41	16-bit Linear	64K	80x30	8x16	640x480	50.350	31.5	60
41	16-bit Linear	64K	80x30	8x16	640x480	63.000	37.9	72
41	16-bit Linear	64K	80x30	8x16	640x480	63.000	37.5	75
42	15-bit Linear	32K	100x37	8x16	800x600	72.000	35.1	56
42	15-bit Linear	32K	100x37	8x16	800x600	80.000	37.9	60
43	16-bit Linear	64K	100x37	8x16	800x600	72.000	35.1	56
43	16-bit Linear	64K	100x37	8x16	800x600	80.000	37.9	60
50	24-bit Linear	16M	80x30	8x16	640x480	75.525	31.5	60
60	Text	16	132x25	8x16	1056x400	41.500	31.5	70
61	Text	16	132x50	8x8	1056x400	41.500	31.5	70
6A/70	Planar	16	100x37	8x16	800x600	36.000	35.1	56
6A/70	Planar	16	100x37	8x16	800x600	40.000	37.9	60
6A/70	Planar	16	100x37	8x16	800x600	50.350	48.1	72
6A/70	Planar	16	100x37	8x16	800x600	49.500	46.9	75
72 I/72 I	Planar	16	128x48	8x16	1024x768	44.900	35.5	43

Mode# (Hex)	Display Mode	Colors	Text Display	Font Size	Pixel Resolution	DotClock (MHz)	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
72/75	Planar	16	128x48	8x16	1024x768	65.000	48.4	60
72 I/72 I	Planar	16	128x48	8x16	1024x768	75.525	57.5	70
72/75	Planar	16	128x48	8x16	1024x768	78.750	60.0	75
78	Packed Pixel	256	80x25	8x16	640x400	25.175	31.5	70
79	Packed Pixel	256	80x30	8x16	640x480	25.175	31.5	60
79	Packed Pixel	256	80x30	8x16	640x480	31.500	37.9	72
79	Packed Pixel	256	80x30	8x16	640x480	31.500	37.5	75
7C	Packed Pixel	256	100x37	8x16	800x600	36.000	35.1	56
7C	Packed Pixel	256	100x37	8x16	800x600	40.000	37.9	60
7C	Packed Pixel	256	100x37	8x16	800x600	50.350	48.1	72
7C	Packed Pixel	256	100x37	8x16	800x600	49.500	46.9	75
7E I	8-bit Linear	256	128x48	8x16	1024x768	44.900	35.5	43
7E	8-bit Linear	256	128x48	8x16	1024x768	65.000	48.4	60
7E	8-bit Linear	256	128x48	8x16	1024x768	75.525	57.5	70
7E	8-bit Linear	256	128x48	8x16	1024x768	78.750	60.00	75

NOTES:
(1) "I" modes are interlaced.

6.27.9 Video Resolution, Colors, Refresh & Clocks Support – CRT, & TFT Panels

Resolution and Color Depth supported for CRT displays and/or TFT panels are contained in this section. In the following table, a representative list of the most memory bandwidth intensive resolution and color depth combinations and of the maximum screen refresh frequencies is provided. The table applies for both CRT and TFT panels, including simultaneous CRT and TFT operation. This list is not a complete list of all modes that the VGA BIOS can support. Refer to the Chips VGA BIOS documentation for more information about VGA BIOS mode support, see section 2.1.

Table 15 Video Resolution, Colors, Refresh, & Clocks Support – CRT, & TFT Panels

Resolution and Color Depth [1]	Screen Refresh [2]	Horiz. Freq.	Dot Clock	Notes
640 x 480 x 8 bpp	85 Hz	43.3 KHz	36 MHz	
640 x 480 x 16 bpp	85 Hz	43.3 KHz	36 MHz	
640 x 480 x 24 bpp	85 Hz	43.3 KHz	36 MHz	
800 x 600 x 8 bpp	85 Hz	53.7 KHz	56.25 MHz	
800 x 600 x 16 bpp	85 Hz	53.7 KHz	56.25 MHz	
800 x 600 x 24 bpp	60 Hz	37.9 KHz	40 MHz	[3]
1024 x 768 x 8 bpp	85 Hz	68.7 KHz	94.5 MHz	
1024 x 768 x 16 bpp	56 Hz	45.2 KHz	60.7 MHz	[3]
1280 x 1024 x 8 bpp	60 Hz	64 KHz	108 MHz	

NOTES
(1) Table contents provided by the document, "Chips HiQVideo Series Mode Support", Application Note AN89, Revision 1.4, Feb 1996. Refer to the document for a list that includes all combinations supported. Except for the interlaced modes in this table, all modes apply to both CRT displays and to TFT panels, including simultaneous CRT and TFT operation.
(2) This is the maximum supported Screen Refresh frequency for the corresponding Resolution and Color Depth
(3) Mode slightly exceeds the computed bandwidth of the main display memory. However, the mode may still be supported depending on final silicon characterization and testing. Support may be possible with second-order software adjustments in the programming of the internal registers and/or somewhat reduced memory bandwidth available for CPU accesses.

6.27.10 Video Resolution, Colors, and Refresh Support – STN-DD Panels

In the following tables, a representative list of the most memory bandwidth intensive resolution and color depth combinations and of the maximum screen refresh frequencies is provided for each STN-DD panel type. Video overlay does not apply to the PC/II+dL video interface. See notes for support of simultaneous CRT & panel operation. This list is not a complete list of all modes that the VGA BIOS can support – please refer to the Chips VGA BIOS documentation for more information about VGA BIOS mode support, see section 2.1.

Table 16 Video Resolution, Colors & Refresh Support – STN-DD Panels

Resolution and Color Depth [1]	Screen Refresh					
	640x480 Color	640x480 Mono	800x600 Color	800x600 Mono	1024x768 Color	1024x768 Mono
640 x 480 x 8 bpp	75 Hz	75 Hz	75 Hz	75 Hz	70 Hz	70 Hz
640 x 480 x 16 bpp	85 Hz	75 Hz	75 Hz	75 Hz	70 Hz [4]	70 Hz
640 x 480 x 24 bpp	75 Hz [3]	75 Hz	75 Hz [3,4]	75 Hz [3,4]	70 Hz [5]	70 Hz [5]
800 x 600 x 8 bpp	75 Hz	75 Hz	85 Hz	75 Hz	70 Hz [3]	70 Hz
800 x 600 x 16 bpp	75 Hz	75 Hz	85 Hz [4]	75 Hz [3]	70 Hz [3,4]	70 Hz [3,4]
800 x 600 x 24 bpp	75 Hz [3]	75 Hz	85 Hz [5]	75 Hz [5]	70 Hz [3,5]	70 Hz [5]
1024 x 768 x 8 bpp	75 Hz	75 Hz	75 Hz	75 Hz	70 Hz [5]	70 Hz
1024 x 768 x 16 bpp	75 Hz	75 Hz	75 Hz [4]	75 Hz [3]	70 Hz [5]	70 Hz [5]
1280 x 1024 x 8 bpp	75 Hz	75 Hz	75 Hz	75 Hz	70 Hz [5]	70 Hz

NOTES

[1] Table contents provided by the document, "Chips HiQVideo Series Mode Support", Application Note AN89, Revision 1.4, Feb 1996. Refer to the document for a list that includes all combinations supported. Unless otherwise noted (see [4,5]), simultaneous CRT and STN-DD panel operation is supported.

[2] This is the maximum supported Screen Refresh frequency for the corresponding Resolution and Color Depth

[3] Mode slightly exceeds the computed bandwidth of the main display memory. However, the mode may still be supported depending on final silicon characterization and testing. Support may be possible with second-order software adjustments in the programming of the internal registers and/or somewhat reduced memory bandwidth available for CPU accesses.

[4] Simultaneous CRT and panel operation is not supported. Panel-only operation can be supported (see note [5] below).

[5] For panels, graphics raster registers and DCLK must be programmed for half the specified refresh rate, and frame acceleration must be enabled to achieve the specified panel FLM frequency. Simultaneous operation with a CRT is not supported.

[6] STN-DD panels require additional buffering compared to TFT panels and CRT displays. STN-DD panels usually are divided into upper and lower half-panels, which must be refreshed simultaneously. A "DD" buffer allows pixels to be read from display memory in a single-scan manner while refreshing the STN-DD panel in a dual-drive ("DD") manner. In the PC/II+dL, the DD buffer is embedded in the main display memory in an off-screen area. In this case, the DD buffer can be either full-frame or half-frame. With a half-frame DD buffer, the refresh rate of the STN-DD panel (FLM frequency) is double the refresh rate of the CRT. This doubling effect is also referred to as frame acceleration. In all of the STN-DD mode listed, frame acceleration can be used to achieve a panel refresh rate twice as high as the specified refresh rate, except in cases where frame acceleration is already assumed to be enabled.

6.28 Watchdog & Power Monitor

The PC/II+dL contains a DS1706S Microprocessor Supervisor that provides a optional Watchdog timer.

For order information for the Watchdog options, see section 10.3.16.

The Watchdog WDS# output is tied to RST# causing a minimum 200 microsecond CPU reset to occur when the watchdog timer triggers. A jumper (JP01) is included between WDS# and RST# to permanently disable the watchdog function (remove jumper's shunt to disable Watchdog, install jumper's shunt to enable watchdog function).

At the hardware level, the Watchdog input must be driven low periodically, at a ***minimum rate of once per second***, to prevent the watchdog WDS# output from being activated. This hardware strobe is normally driven (by default) by the PC/II+dL board hardware, and in this mode, the watchdog does not trigger, and the Watchdog timer is in inactive mode.

To allow the Watchdog timer to trigger and cause a CPU reset, the Watchdog jumper must be inserted, the Watchdog must be activated by calling BIOS Int 15h, function 0FE00h, and the Watchdog strobe must not have been issued (BIOS Int 15h, function 0FDh) for a duration of 1 second.

The program-accessible interface to the Watchdog Activate/Deactivate control signal and the Watchdog Strobe signal are provided by the PC/II+dL BIOS Int 15h (functions 0FEH and 0FDh respectively), as described in the following subsections.

1. FUNCTION 0FEh – ACTIVATE AND DEACTIVATE WATCHDOG TIMER

This function activates the watchdog timer to allow software control of strobing, or deactivates the watchdog timer to disable watchdog functionality.

In ACTIVE mode the watchdog will trigger and cause a CPU reset if the watchdog jumper is inserted and a software strobe has not been issued to the watchdog in the last second using function 0FDh. Therefore, strobing at a one strobe per second rate or faster is required.

In INACTIVE mode strobing is not required and the watchdog will **not** cause a CPU reset to occur. This is the default at boot time.

```
MOV    AH,0FEh
MOV    AL,<Command>                    00h = ACTIVATE watchdog
                                       01h = DEACTIVATE watchdog
INT    15h
-- returns here after the specified watchdog MODE has been entered
       / ALL Registers are preserved
```

2. FUNCTION 0FDh – STROBE WATCHDOG TIMER

This function strobes the watchdog timer, causing its timer to restart. In ACTIVE mode (see function 0FEh), the watchdog must be strobed at a one strobe per second rate, and preferably at a faster rate, to prevent the watchdog timer from expiring and a CPU reset from occurring. In INACTIVE mode this function has no affect.

```
MOV    AH,0FDh
INT    15h
-- returns here after one strobe has been issued to the watchdog
       / ALL Registers are preserved
```


7 System Resource Maps

7.1 I/O Address Map

Table 17 I/O Map

I/O ADDRESS REGION [1]	USED BY	DESCRIPTION	USED FOR
0000-000F	ACC2089	DMA controller 1	8237A-5
0020-0021	ACC2089	Interrupt controller 1	8259A-MASTER
0040-0043	ACC2089	Timer	8254
0060,0064	ACC2089	Keyboard controller	
0070-0071	ACC2089	Real-time clock, NMI mask	DS1685
0080-008F	ACC2089	DMA page register	74LS612
0092	ACC2089	Alternate gate a20, fast reset register	
00A0-00A1	ACC2089	Interrupt controller 2	8259A-SLAVE
00C0-00DF	ACC2089	DMA controller 2	8237A-5
00F0	ACC2089	Clear math coprocessor busy	
00F1	ACC2089	Reset math coprocessor	
00F2	ACC2089	ACC2089 configuration register index	BIOS
00F3	ACC2089	ACC2089 configuration register data	BIOS
00F8-00FF	ACC2089	Math coprocessor	
0102	65550	VGA global enable	
0140-015F	AIC6360	SCSI-2 controller – primary	Scsi I/O
0170-0177	ACC2089	Secondary HDC	
0180-019F	CPLD	Reserved	
01F0-01F7	ACC2089	Primary HDC	IDE
0200-0207		Reserved	Game Port 1
0238-023B		Reserved	Bus Mouse
0238-023F		Reserved	Alternate Bus Mouse
0278-027F		Reserved	Printer #2
02B0-02DF		Reserved	Video – EGA
02E0-02E7		Reserved	GPIB
02E8-02EF	PC97338	COM4-IRQ3	Serial I/O – #4
02F8-02FF	ACC2089	COM2-IRQ3	Serial I/O – #2
0300-030F	CS8900	Ethernet controller	Ethernet
0300-031F		Reserved	Prototype Cards
0340-035F	AIC6360	SCSI-2 controller – secondary	Scsi I/O
0370-0377	ACC2089	Secondary FDC	
0378-037A	ACC2089	LPT1 (Standard mode)	Printer #1
037B-037F	ACC2089	LPT1 (EPP mode)	Printer #1 – EPP

I/O ADDRESS REGION [1]	USED BY	DESCRIPTION	USED FOR
0398-0399	PC97338	PC97338 configuration register index-data	BIOS
03B4-03B5	65550	VGA crtc index / data	VGA BIOS
03BA	65550	VGA status register / Feature Control Register	VGA BIOS
03BD	PC97338	PNP (Plug & Play)	PNP Initialization
03C0-03C1	65550	VGA attrib controller index / data	VGA BIOS
03C2	65550	VGA input status register 0 / MSR	VGA BIOS
03C3	65550	VGA motherboard video system enable	VGA BIOS
03C4-03C5	65550	VGA sequence index / data	VGA BIOS
03C6-03C9	65550	VGA color palette registers	VGA BIOS
03CA	65550	VGA feature control register	VGA BIOS
03CC	65550	VGA misc output register	VGA BIOS
03CE-03CF	65550	VGA graphics controller index/data	VGA BIOS
03D0-03D1	65550	Video flat panel extension regs index/data	VGA BIOS
03D2-03D3	65550	Video multimedia extension regs index/data	VGA BIOS
03D4-03D5	65550	VGA CRTC index/data (CGA emulation)	VGA BIOS
03D6-03D7	65550	Video configuration extensions data/index	VGA BIOS
03DA	65550	VGA status register	VGA BIOS
03E8-03EF	PC97338	COM3-IRQ4	Serial I/O – #3
03F0-03F7	ACC2089	Primary FDC	Floppy
03F8-03FF	ACC2089	COM1-IRQ4	Serial I/O – #1
0778-077A	ACC2089	LPT1 (ECP mode)	Printer #1 – ECP

NOTES
[1] *Addresses are expressed in hexadecimal notation; all addresses are in the 65K physical I/O address space supported by the processor.*

7.2 Memory Map

Table 18 Memory Map

MEMORY ADDRESS REGION [1]	LENGTH	DESCRIPTION
0x00000000 – 0x0009FFFF	640 KB	Base Memory Address Region.
0x000A0000 – 0x000AFFFF	64 KB	Video 65550 – VGA Frame Buffer
0x000B0000 – 0x000B7FFF	32 KB	Video 65550 – MDA Emulation Character Buffer
0x000B8000 – 0x000BFFFF	32 KB	Video 65550 – CGA Emulation Frame Buffer
0x000C0000 – 0x000CFFFF	64 KB	Option BIOS Memory Address Region. This memory address region is ALWAYS shadowed. All memory accesses to this region are always forwarded to system memory, never to the system bus. This region typically contains the VGA BIOS.
0x000D0000 – 0x000DFFFF	64 KB	Flash Memory Address Region (for accessing any 1 of 128- 64K flash sectors). This memory address region is used to access both User Flash pages and Bios Flash pages. It can be shadowed with system memory when access to Flash is not required. Memory accesses are forwarded to the system bus, causing FCS (Flash Chip Select) to be asserted, only if the Flash Window is enabled The page numbers are assigned as follows: page 0 – 127 User flash array page 128 – 131 BIOS flash
0x000E0000 – 0x000E7FFF	32 KB	Reserved.
0x000E8000 – 0x000EFFFF	32 KB	Disk-on-Chip Memory Address Region. This memory address region is used to access the Disk-On-Chip, and it can be shadowed with system memory when access to Disk-On-Chip is not required. Memory accesses are forwarded to the system bus, causing X32CS# (Disk-on-Chip Chip Select) to be asserted only if X32CS is enabled.
0x000F0000 – 0x000FFFFF	64 KB	BIOS ROM Memory Address Region. This memory address region is used for standard BIOS ROM. Memory write accesses to this address region are always forwarded to system memory, never to the system bus. Memory read accesses to this address region are forwarded to the system bus, only if enabled, otherwise they are forwarded to system memory.
0x00100000 – 0x01FFFFFF	31 MB	Additional Extended Main Memory (by option)
0x02000000 – 0x027FFFFF	8 MB	Video 65550 – Linear Accessible Buffer. This memory region always resides higher than the last main memory address, usually at the 32 MB boundary for the PC/II+dL. ***Video BIOS will set the actual address used, which may be higher or lower than at the 32 MB boundary.***

NOTES
[1] Addresses are expressed in hexadecimal notation
[2] Please refer to the ACC 2089 Datasheet for information on the DRAM memory controller.

7.2.1 Memory Shadowing

The Shadowing options for EDO DRAM are controlled by register 02h in the 2089. These functions are described below. Please refer to the ACC 2089 data sheet for further details.

7.2.2 Shadow Disable

After a power-up or a system reset, all shadowing is disabled. Therefore any memory accesses to the area from 000C0000 – 000FFFFF is directed to the system bus.

7.2.3 Shadow Enable

Shadowing may be enabled on a 64K-page basis for each of the 64 KB pages beginning at C0000, D0000, E0000 and F0000. When shadowing is enabled, both read and write operations are directed to DRAM rather than to the system bus.

7.2.4 Shadow Protection

In addition, there is a single write-enable bit, which can inhibit write operations to shadow RAM. If a memory region is not shadowed, then both read and write operations are forwarded to the bus. Both the X32 (flash disk – Disk-on-Chip®) device and the User Flash Array device have enable bits, which allow the corresponding chip select to be disabled.

7.3 Interrupt IRQ Map

Table 19 Interrupt Map

INT. REQ. NUMBER (NOTE 4)	DEFAULT SOURCE in PC/II+dx		PC/104 BUS		COM3 & COM4 (NOTE 6)	ETHERNET (NOTE 7)
	SOURCE COMP.	DESCRIPTION	CONNECTOR PIN	PC/104 BUS NOTES		
IRQ0	ACC2089	TIMER 0	-			
IRQ1	ACC2089	Integrated KEYBOARD	-			
IRQ2	ACC2089	Cascade to Int Controller 2	-			
IRQ3	ACC2089	Integrated COM2	-	1		
IRQ4	ACC2089	Integrated COM1	-	1		
IRQ5	-	-	J001.B23		COM3/4	ETHERNET
IRQ6	ACC2089	Integrated FDC	-	1		
IRQ7	ACC2089	Integrated LPT1	J001.B21		COM3/4	
IRQ8	DS1685	Real Time Clock – Timer/Alarm	-		COM3/4	
IRQ9	-	-	J001.B4		COM3/4	
IRQ10	CS8900	ETHERNET (IRQs 5,9,10)	J002.D3	3, 5	COM3/4	ETHERNET
IRQ11	AIC6360	SCSI	J002.D4	3, 5	COM3/4	ETHERNET
IRQ12	ACC2089	Integrated PS/2 MOUSE	-	1		
IRQ13	-	(Numeric Coprocessor)	-			
IRQ14	ACC2089	Integrated IDE	J002.D7	2, 5		
IRQ15	-	-	J002.D6			

NOTES

[1] Not available on PC/104 bus;
IRQ12 is dedicated to the on-board keyboard controller (Mouse device).
IRQ3 and IRQ4 are dedicated to the ACC 2089 serial channels COM1 and COM2.
IRQ6 is dedicated to the ACC 2089 floppy disk controller.

[2] IRQ14 is available on the PC/104 bus when IDE has been disabled within the ACC 2089 controller.

[3] IRQ10 and IRQ11 are available on the PC/104 bus when ETHERNET and SCSI options are not installed or have been assigned another IRQ for their use.

[4] Interrupt request numbers are enumerated from 0 through 15 per the conventional AT standard. Interrupt request levels are numbered 0 through 7 in each physical 8259A interrupt controller. The interrupt controllers are tied together through interrupt level 2 of control #1 (that is, interrupt pending requests are presented from interrupt controller #2 to level 2 of interrupt controller #1). The physical implementation of interrupt controllers is internal to the ACC 2089. This implementation mirrors the implementation of two 8259A controllers, so that the interface is identical to the AT standard. When an interrupt is pending for IRQ8–IRQ15, the interrupt is in-service in both controllers, in controller #1 at level 2, and controller #2 at level 0–7; both controllers are normally acknowledged after service completes to clear the pending interrupt, per the standard AT standard.

[5] Requires verification by megatel for your particular configuration.

[6] COM3 & COM4 are supported by the National 97338 Plug&Play functionality; interrupts noted are least likely to cause conflicts in typical PC/II+dL configurations.

[7] ETHERNET is supported by the configuration utility for the CS8900. For more information contact megatel engineering.

7.4 DMA Channel Map

Table 20 DMA Map

DMA REQ. NUMBER (NOTE 1)	DEFAULT SOURCE in PC/II+dx		PC/104 BUS		COM4 (PnP) (NOTE 3)	ETHERNET (NOTE 4,5)
	SOURCE	DESCRIPTION	CONNECTOR PIN	PC/104 BUS NOTES		
DRQ0			J002.D9		COM4	-
DRQ1			J001.B18		COM4	-
DRQ2	ACC2089	Integrated FDC		2	-	-
DRQ3			J001.B16		COM4	-
DRQ4	ACC2089	Cascade	-		-	-
DRQ5			J002.D11		-	ETHERNET
DRQ6	AIC6360	SCSI	J002.D13	5	-	ETHERNET
DRQ7			J002.D15		-	ETHERNET

NOTES
[1] DMA request numbers are enumerated from 0 through 7 per the conventional AT standard. Two DMA controllers, the first containing four 8-bit channels (0–3 – DRQ0–DRQ3) is cascaded to channel 0 of the second controller (DRQ4). Controller #2 contains four 16-bit channels.
[2] DRQ2 is dedicated to the ACC 2089 Floppy Controller.
[3] DRQ0, DRQ1 & DRQ3 are supported by the National 97338 Plug&Play functionality; DMA requests noted are least likely to cause conflicts in typical PC/II+dx configurations. Contact megatel for assistance on using these DMA requests on COM4.
[4] ETHERNET is supported by the configuration utility for the CS8900. For more information contact megatel engineering.
[5] DRQ6 is available on the PC/104 bus when SCSI option is not installed or SCSI has been configured not to use the DMA channel.
[6] Requires verification by megatel for your particular configuration.

8 Connector Pinouts

This section contains pinout and signal description details for each connector on the PC/II+dx.

You can link to the pinout information for any connector, using the table below.

INDEX OF PINOUTS			
CONNECTOR		**DESCRIPTION**	**See**
J001,J002		PC/104 Connectors AB and CD	Section 8.1
J003,J004		Mass I/O Connectors (165-pin 2-mm 5X33 grid)	Section 8.2
	J003,J004	Power & Miscellaneous	Section 8.2.1
	J003	IDE Interface	Section 8.2.2
		SCSI Bus Interface	Section 8.2.14
		Video CRT Interface	Section 8.2.15
	J004	Serial COM1 Interface	Section 8.2.3
		Serial COM2 Interface	Section 8.2.4
		Serial COM3 Interface	Section 8.2.5
		Serial COM4 Interface	Section 8.2.6
		Floppy Disk Interface	Section 8.2.7
		Keyboard Interface	Section 8.2.9
		Mouse Interface	Section 8.2.10
		Panel Interface	Section 8.2.8
		Parallel Printer Interface	Section 8.2.13
		Reset Interface	Section 8.2.11
		Speaker Output Interface	Section 8.2.12
J005		Ethernet Connector	Section 8.3
J007		Power Connector (+5V)	Section 8.4
J008		Fan Connector	Section 8.5
J010		Power Connector (+3.3V)	Section 8.6

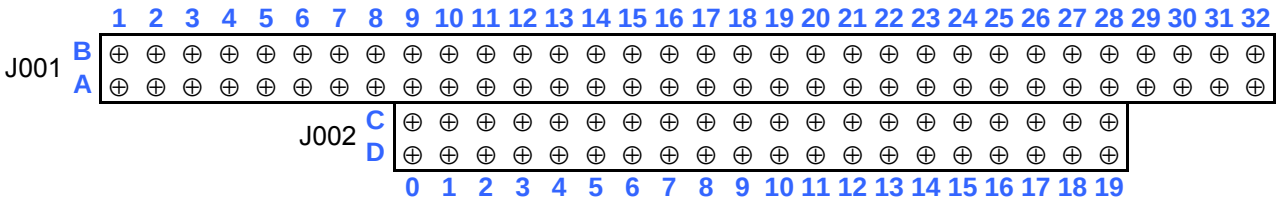
8.1 Pinout of J001, J002 – PC/104 Connectors AB and CD

The PC/II+dL board supports a 64-pin (2x32) PC/104 AB Bus connector (J001), and a 40-pin (2x20) PC/104 CD Bus connector (J002).

Please refer to the PC/104 Specification document for a complete description of these connectors; see the reference documents section 2.3.

For ordering information, see section 10.3.17.
For part number information, see section 6.7.

Figure 4 Diagram – PC/104 J001(A–B), J002 (C–D) – 2X32 .100" Header



NOTES
1 *Top (component) view is shown.*
2 *J001 numbering begins with 1, but J002 numbering begins with 0 (per PC/104 spec...)*
3 *J001 top row (as shown) is labeled "A", but J002 top row is labeled "C" (per PC/104 spec...)*
4 *Grid spacing in X-Y direction is .100 inch; Grid spacing between J001-A and J002-C is .100 inch.*

.

Table 21 Pinout – PC/104 J001 (Rows A and B) – 2 X 32 .100" Header

PIN GROUP [1,3]	PIN [2]	ROW A	ROW B
PC104 – AB	1	IOCHCHK*	0V
PC104 – AB	2	SD7	RESETDRV
PC104 – AB	3	SD6	+5V
PC104 – AB	4	SD5	IRQ9
PC104 – AB	5	SD4	-5V
PC104 – AB	6	SD3	DRQ2
PC104 – AB	7	SD2	-12V
PC104 – AB	8	SD1	ENDXFR*
PC104 – AB	9	SD0	+12V
PC104 – AB	10	IOCHRDY	(KEY) [3]
PC104 – AB	11	AEN	SMEMW*
PC104 – AB	12	SA19	SMEMR*
PC104 – AB	13	SA18	IOW*
PC104 – AB	14	SA17	IOR*
PC104 – AB	15	SA16	DACK3*
PC104 – AB	16	SA15	DRQ3
PC104 – AB	17	SA14	DACK1*
PC104 – AB	18	SA13	DRQ1
PC104 – AB	19	SA12	REFRESH*
PC104 – AB	20	SA11	SYSCLK
PC104 – AB	21	SA10	IRQ7
PC104 – AB	22	SA9	IRQ6
PC104 – AB	23	SA8	IRQ5
PC104 – AB	24	SA7	IRQ4
PC104 – AB	25	SA6	IRQ3
PC104 – AB	26	SA5	DACK2*
PC104 – AB	27	SA4	TC
PC104 – AB	28	SA3	BALE
PC104 – AB	29	SA2	+5V
PC104 – AB	30	SA1	OSC
PC104 – AB	31	SA0	0V
PC104 – AB	32	0V	0V

NOTES
(1) Refer to the PC/104 Specification.
(2) Pin numbering complies with the PC/104 Specification, which is also used on the PC/II+dL board. Refer to the connector diagram in this section.
(3) Rows C and D are not required on 8-bit modules. B10 and C19 are key locations. Signal timing and function are as specified in the P996 Specification. Signal source/sink currents differ from P996 values.

Table 22 Pinout – PC/104 J002 (Rows C and D) – 2 X 20 .100" Header

PIN GROUP [1,3]	PIN [2]	ROW C	ROW D
PC104 – CD	0	0V	0V
PC104 – CD	1	SBHE*	MEMCS16*
PC104 – CD	2	LA23	IOCS16*
PC104 – CD	3	LA22	IRQ10
PC104 – CD	4	LA21	IRQ11
PC104 – CD	5	LA20	IRQ12
PC104 – CD	6	LA19	IRQ15
PC104 – CD	7	LA18	IRQ14
PC104 – CD	8	LA17	DACK0*
PC104 – CD	9	MEMR*	DRQ0
PC104 – CD	10	MEMW*	DACK5*
PC104 – CD	11	SD8	DRQ5
PC104 – CD	12	SD9	DACK6*
PC104 – CD	13	SD10	DRQ6
PC104 – CD	14	SD11	DACK7*
PC104 – CD	15	SD12	DRQ7
PC104 – CD	16	SD13	+5V
PC104 – CD	17	SD14	MASTER*
PC104 – CD	18	SD15	0V
PC104 – CD	19	(KEY) [3]	0V

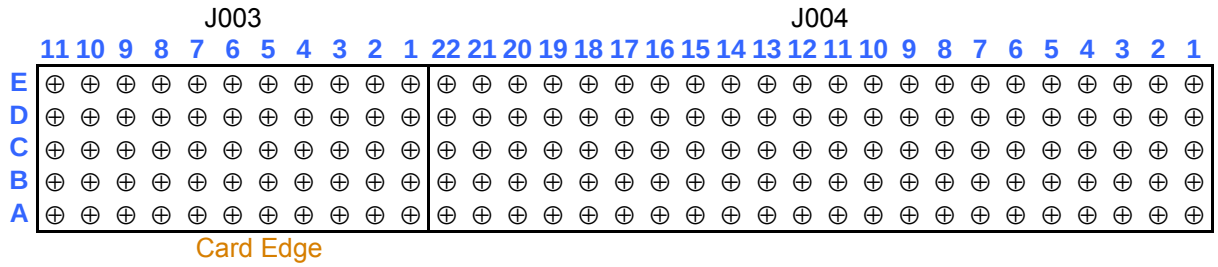
NOTES
(1) Refer to the PC/104 Specification.
(2) Pin numbering complies with the PC/104 Specification, which is also used on the PC/II+dL board. Refer to the connector diagram in this section.
(3) Rows C and D are not required on 8-bit modules. B10 and C19 are key locations. Signal timing and function are as specified in the P996 Specification. Signal source/sink currents differ from P996 values.

8.2 Pinout of J003, J004 – Mass I/O Connector

All peripheral I/O, with the exception of Ethernet (J005), is pulled from the PC/II+dL board to a 5 X 33 2mm grid Mass I/O Connector. The Mass I/O Connector is normally provided using two separate connectors, J003, a 5 X 11 2-mm connector, and J004, a 5 X 22 2-mm connector. The PC/II+dL board can be ordered with either, both or none of these two connectors installed, although both would be installed in a typical case. In addition, the PC/II+dL board can be shipped with any combination of user-specified 2-mm headers.

For order information, see sections 10.3.18 and 10.3.19.
For part number information, see section 6.7.

Figure 5 Diagram – MASS I/O J003, J004 (Rows A–E) – 5X11, 5X22 2-mm HM Connector



NOTES
(1) Top (component) view is shown. This is the view when facing a either a straight connector from the top, or a right-angle connector facing the outer side (the mating side).

Table 23 Pinout – MASS I/O J003 (Rows A, B, C, D and E) – 5 X 11 2mm HM Connector

PIN GROUP	POS	ROW e	ROW d	ROW c	ROW b	ROW a
V1-VIDEO1 – CRT1	1	V1-R	V1-G	V1-B	V1-HSYNC	V1-VSYNC
A1-IDE1	2	A1-DD7	A1-DD8	A1-DD6	A1-DD9	A1-DD5
A1-IDE1	3	A1-DD10	A1-DD4	A1-DD11	A1-DD3	A1-DD12
A1-IDE1	4	A1-DD2	A1-DD13	A1-DD1	A1-DD14	A1-DD0
A1-IDE1	5	A1-DD15	A1-DMARQ	A1-DIOW#	A1-DIOR#	A1-IORDY
A1-IDE1	6	A1-DMACK#	A1-INTRQ	A1-IOCS16#	A1-DA1	A1-DA0
A1-IDE1 S1-SCSI	7	A1-DA2	A1-CS0#	A1-CS1#	S1-REQ#	S1-MSG#
S1-SCSI	8	S1-C/D#	S1-I/O#	S1-RST#	S1-ATN#	S1-AKN#
S1-SCSI	9	S1-BSY#	S1-SEL#	S1-DP#	S1-D0#	S1-D1#
S1-SCSI	10	S1-D2#	S1-D3#	S1-D4#	S1-D5#	S1-D6#
POWER	11	S1-D7#	GND	GND	+5V	+5V

Table 24 Pinout – MASS I/O J004 (Rows A, B, C, D and E) – 5 X 22 2mm HM Connector

PIN GROUP	POS	ROW e	ROW d	ROW c	ROW b	ROW a
L1-PANEL	1	L1-FPD23	L1-FPD22	GND	L1-FPD21	+5V
L1-PANEL	2	L1-FPD20	L1-FPD19	L1-FPD18	L1-FPD17	L1-FPD16
L1-PANEL	3	L1-FPD15	L1-FPD14	L1-FPD13	L1-FPD12	L1-FPD11
L1-PANEL	4	L1-FPD10	L1-FPD9	L1-FPD8	L1-FPD7	L1-FPD6
L1-PANEL	5	L1-FPD5	L1-FPD4	L1-FPD3	L1-FPD2	L1-FPD1
L1-PANEL	6	L1-FPD0	L1-SHFCLK	L1-LP	L1-FLM	L1-ENAVEE
L1-PANEL MS-SPEAKER	7	L1-ENAVDD	L1-M	L1-ACT	L1-ENABKL	MS-SPKOUT
MR-RESET MISCELLANEOUS K1-KEYBOARD	8	MR-RSTSW	PWRGOOD	K1-DAT	K1-CLK	+3.3V
M1-MOUSE P1-PARALLEL1 – LPT1	9	M1-DAT	M1-CLK	P1-STB#	P1-AFD#	P1-D0
P1-PARALLEL1 – LPT1	10	P1-ERR#	P1-D1	P1-INIT#	P1-D2	P1-SLIN#
P1-PARALLEL1 – LPT1	11	P1-D3	P1-D4	P1-D5	P1-D6	P1-D7
P1-PARALLEL1 – LPT1 C1-SERIAL1 – COM1	12	P1-AKN#	P1-BUSY	P1-PE	P1-SLCT	C1-DCD
C1-SERIAL1 – COM1	13	C1-DSR	C1-RXD	C1-RTS	C1-TXD	C1-CTS
C1-SERIAL1 – COM1 C2-SERIAL2 – COM2	14	C1-DTR	C1-RI	C2-DCD	C2-DSR	C2-RXD
C2-SERIAL2 – COM2	15	C2-RTS	C2-TXD	C2-CTS	C2-DTR	C2-RI
C3-SERIAL3 – COM3	16	C3-DCD	C3-DSR	C3-RXD	C3-RTS	C3-TXD
C3-SERIAL3 – COM3 C4-SERIAL4 – COM4	17	C3-CTS	C3-DTR	C3-RI	C4-DCD	C4-DSR
C4-SERIAL4 – COM4	18	C4-RXD	C4-RTS	C4-TXD	C4-CTS	C4-DTR
C4-SERIAL4 – COM4	19	C4-RI	Rsvd	Rsvd	Rsvd	Rsvd
F1-FLOPPY1	20	F1-DENSL0#	F1-INDEX#	F1-MTR0#	F1-DS1#	F1-DS0#
F1-FLOPPY1	21	F1-MTR1#	F1-DIR#	F1-STEP#	F1-WDATA#	F1-WGATE#
F1-FLOPPY1	22	F1-TRK0#	F1-WP#	F1-RDATA#	F1-HDSEL#	F1-DKCHG#

8.2.1 Pinout of J003,J004 – Mass I/O – Power & Miscellaneous (J003,J004)

Table 25 Signals – Mass I/O J003,J004 – Power & Miscellaneous

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
+3.3V	J004-a8	+3.3v	Power +3.3 V Use only for sourcing +3.3 V to QTB boards from CPU board.
+5V	J004-a1	+5V	Power +5 V. Use only for sourcing +5 V to QTB boards from CPU board.
+5V	J003-b11	+5V	Power +5 V. Use only for sourcing +5 V to QTB boards from CPU board.
+5V	J003-a11	+5V	Power +5 V. Use only for sourcing +5 V to QTB boards from CPU board.
GND	J004-c1	Ground	Ground
GND	J003-d11	Ground	Ground
GND	J003-c11	Ground	Ground
PWRGOOD	J004-d8	Power Good	This Active High signal is the Power Good output signal. It pulses low for 200 ms (typical, minimum 130 ms) when triggered by RSTSW# or by a Watchdog Timer Expired event, and it remains low whenever VCC is below the reset threshold or when the RSTSW# signal input is a logic low. This output signal remains low for 200ms (typical, minimum 130 ms) after one of the following occurs: VCC rises above the reset threshold, the watchdog triggers a reset, or the RSTSW# input signal goes low to high.

8.2.2 Pinout of J003,J004 – Mass I/O – IDE (J003)

For more information on the IDE features, see section 6.25.
For order information, see sections 10.3.8 and 10.3.18.

Table 26 Signals – Mass I/O J003,J004 – IDE Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
A1-DA0	J003-a6	Address Bus 0	This signal is Address Bit 0 of the ATA Address Bus that is connected to IDE Channel.
A1-DA1	J003-b6	Address Bus 1	This signal is Address Bit 1 of the ATA Address Bus that is connected to IDE Channel.
A1-DA2	J003-e7	Address Bus 2	This signal is Address Bit 2 of the ATA Address Bus that is connected to IDE Channel.
A1-CS0#	J003-d7	Chip Select 1 for Ch 0	This is the Chip Select 1 command output pin to enable the IDE device to watch the Read/Write Command.
A1-CS1#	J003-c7	Chip Select 3 for Ch 1	This is the Chip Select 3 command output pin to enable the IDE device to watch the Read/Write Command.
A1-DD0	J003-a4	Data Bus 0	This signal is Data Bit 0 of the Data Bus that is connected to IDE Channel.
A1-DD1	J003-c4	Data Bus 1	This signal is Data Bit 1 of the Data Bus that is connected to IDE Channel.
A1-DD2	J003-e4	Data Bus 2	This signal is Data Bit 2 of the Data Bus that is connected to IDE Channel.
A1-DD3	J003-b3	Data Bus 3	This signal is Data Bit 3 of the Data Bus that is connected to IDE Channel.
A1-DD4	J003-d3	Data Bus 4	This signal is Data Bit 4 of the Data Bus that is connected to IDE Channel.
A1-DD5	J003-a2	Data Bus 5	This signal is Data Bit 5 of the Data Bus that is connected to IDE Channel.
A1-DD6	J003-c2	Data Bus 6	This signal is Data Bit 6 of the Data Bus that is connected to IDE Channel.
A1-DD7	J003-e2	Data Bus 7	This signal is Data Bit 7 of the Data Bus that is connected to IDE Channel.
A1-DD8	J003-d2	Data Bus 8	This signal is Data Bit 8 of the Data Bus that is connected to IDE Channel.
A1-DD9	J003-b2	Data Bus 9	This signal is Data Bit 9 of the Data Bus that is connected to IDE Channel.
A1-DD10	J003-e3	Data Bus 10	This signal is Data Bit 10 of the Data Bus that is connected to IDE Channel.
A1-DD11	J003-c3	Data Bus 11	This signal is Data Bit 11 of the Data Bus that is connected to IDE Channel.
A1-DD12	J003-a3	Data Bus 12	This signal is Data Bit 12 of the Data Bus that is connected to IDE Channel.
A1-DD13	J003-d4	Data Bus 13	This signal is Data Bit 13 of the Data Bus that is connected to IDE Channel.
A1-DD14	J003-b4	Data Bus 14	This signal is Data Bit 14 of the Data Bus that is connected to IDE Channel.

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
A1-DD15	J003-e5	Data Bus 15	This signal is Data Bit 15 of the Data Bus that is connected to IDE Channel.
A1-DIOR#	J003-b5	IO Read Command	This signal is the IOR command output pin that notifies the IDE device to assert the Read Data.
A1-DIOW#	J003-c5	IO Write Command	This signal is the IOW command output pin that notifies the IDE device that the available Write Data is already asserted by the onboard IDE controller.
A1-DMACK#	J003-e6	DACK for IDE Master	This is an output pin that grants the IDE Channel DMA request to begin the IDE Master Transfer. Use of this signal depends upon the type of board.
A1-DMARQ	J003-d5	DMA Request for IDE Master	This is an input pin from the IDE Channel DMA that requests an IDE master transfer. Use of this signal depends upon the type of board.
A1-IOCS16#	J003-c6	Device 16-Bit I-O	This is an input pin from the IDE device which, during PIO transfer modes 0, 1 or 2, indicates to the host system that the 16-bit data port has been addressed and that the device is prepared to send or receive a 16-bit data word.
A1-IORDY	J003-a5	IDE Ready	This is an input pin from the IDE Channel that indicates that the IDE device is ready to terminate the IDE command. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready.
A1-INTRQ	J003-d6	IDE Interrupt	This is an input pin from the IDE Channel that signals an interrupt. It will be routed to the appropriate 8259 interrupt controller input. Depending upon the board type, this input may be steerable to other interrupt levels.

8.2.3 Pinout of J003,J004 – Mass I/O – Serial COM1 (J004)

For more information on the Serial Port features, see section 6.23.
For order information, see sections 10.3.13 and 10.3.19.

Table 27 Signals – Mass I/O J003,J004 – Serial COM1 Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
C1-CTS	J004-a13	Clear to Send	This active low input is the handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of CTSJ signal by reading bit 4 of Modem Status Register (MSR). A CTS signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when CTS changes state. The CTS signal has no effect on the transmitter. Note : Bit 4 of MSR is the complement of CTS.
C1-DCD	J004-a12	Data Carrier Detect	This active low input is a handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of the DCD signal by reading bit 7 of Modem Status Register (MSR). A DCD signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when the DCD input changes state. Note : bit 7 of MSR is the complement of DCD.
C1-DSR	J004-e13	Data Set Ready	This active low input is the handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR signal by reading bit5 of Modem Status Register (MSR). A DSR signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DSR changes state. Note: Bit 5 of MSR is the complement of DSR.
C1-DTR	J004-e14	Data Terminal Ready	This active low output is the handshake output signal that signifies to modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR).
C1-RI	J004-d14	Ring Indicator	This active low input is the handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI signal by reading bit 6 of Modem Status Register (MSR). A RI signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when the RI input changes state. Note : bit 6 of MSR is the complement of RI.
C1-RTS	J004-c13	Request to Send	This Active low output is the handshake output signal that notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS signal to inactive mode (high).
C1-RXD	J004-d13	Receive Data	This input is the receive data serial input line, which carries RS-232 data.
C1-TXD	J004-b13	Transmit Data	This output is the transmit data serial output line, which carries RS-232 data.

8.2.4 Pinout of J003,J004 – Mass I/O – Serial COM2 (J004)

For more information on the Serial Port features, see section 6.23.
For order information, see sections 10.3.13 and 10.3.19.

Table 28 Signals – Mass I/O J003,J004 – Serial COM2 Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
C2-CTS	J004-c15	Clear to Send	This active low input is the handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of CTSJ signal by reading bit 4 of Modem Status Register (MSR). A CTS signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when CTS changes state. The CTS signal has no effect on the transmitter. Note : Bit 4 of MSR is the complement of CTS.
C2-DCD	J004-c14	Data Carrier Detect	This active low input is a handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of the DCD signal by reading bit 7 of Modem Status Register (MSR). A DCD signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when the DCD input changes state. Note : bit 7 of MSR is the complement of DCD.
C2-DSR	J004-b14	Data Set Ready	This active low input is the handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR signal by reading bit5 of Modem Status Register (MSR). A DSR signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DSR changes state. Note: Bit 5 of MSR is the complement of DSR.
C2-DTR	J004-b15	Data Terminal Ready	This active low output is the handshake output signal that signifies to modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR).
C2-RI	J004-a15	Ring Indicator	This active low input is the handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI signal by reading bit 6 of Modem Status Register (MSR). A RI signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when the RI input changes state. Note : bit 6 of MSR is the complement of RI.
C2-RTS	J004-e15	Request to Send	This Active low output is the handshake output signal that notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS signal to inactive mode (high).
C2-RXD	J004-a14	Receive Data	This input is the receive data serial input line, which carries RS-232 data.
C2-TXD	J004-d15	Transmit Data	This output is the transmit data serial output line, which carries RS-232 data.

8.2.5 Pinout of J003,J004 – Mass I/O – Serial COM3 (J004)

For more information on the Serial Port features, see section 6.23.
For order information, see sections 10.3.13 and 10.3.19.

Table 29 Signals – Mass I/O J003,J004 – Serial COM3 Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
C3-CTS	J004-e17	Clear to Send	This active low input is the handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of CTSJ signal by reading bit 4 of Modem Status Register (MSR). A CTS signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when CTS changes state. The CTS signal has no effect on the transmitter. Note : Bit 4 of MSR is the complement of CTS.
C3-DCD	J004-e16	Data Carrier Detect	This active low input is a handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of the DCD signal by reading bit 7 of Modem Status Register (MSR). A DCD signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when the DCD input changes state. Note : bit 7 of MSR is the complement of DCD.
C3-DSR	J004-d16	Data Set Ready	This active low input is the handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR signal by reading bit5 of Modem Status Register (MSR). A DSR signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DSR changes state. Note: Bit 5 of MSR is the complement of DSR.
C3-DTR	J004-d17	Data Terminal Ready	This active low output is the handshake output signal that signifies to modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR).
C3-RI	J004-c17	Ring Indicator	This active low input is the handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI signal by reading bit 6 of Modem Status Register (MSR). A RI signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when the RI input changes state. Note : bit 6 of MSR is the complement of RI.
C3-RTS	J004-b16	Request to Send	This Active low output is the handshake output signal that notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS signal to inactive mode (high).
C3-RXD	J004-c16	Receive Data	This input is the receive data serial input line, which carries RS-232 data.
C3-TXD	J004-a16	Transmit Data	This output is the transmit data serial output line, which carries RS-232 data.

8.2.6 Pinout of J003,J004 – Mass I/O – Serial COM4 (J004)

For more information on the Serial Port features, see section 6.23.
For order information, see sections 10.3.13 and 10.3.19.

Table 30 Signals – Mass I/O J003,J004 – Serial COM4 Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
C4-CTS	J004-b18	Clear to Send	This active low input is the handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of CTSJ signal by reading bit 4 of Modem Status Register (MSR). A CTS signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when CTS changes state. The CTS signal has no effect on the transmitter. Note : Bit 4 of MSR is the complement of CTS.
C4-DCD	J004-b17	Data Carrier Detect	This active low input is a handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of the DCD signal by reading bit 7 of Modem Status Register (MSR). A DCD signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when the DCD input changes state. Note : bit 7 of MSR is the complement of DCD.
C4-DSR	J004-a17	Data Set Ready	This active low input is the handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR signal by reading bit5 of Modem Status Register (MSR). A DSR signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DSR changes state. Note: Bit 5 of MSR is the complement of DSR.
C4-DTR	J004-a18	Data Terminal Ready	This active low output is the handshake output signal that signifies to modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR).
C4-RI	J004-e19	Ring Indicator	This active low input is the handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI signal by reading bit 6 of Modem Status Register (MSR). A RI signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when the RI input changes state. Note : bit 6 of MSR is the complement of RI.
C4-RTS	J004-d18	Request to Send	This Active low output is the handshake output signal that notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS signal to inactive mode (high).
C4-RXD	J004-e18	Receive Data	This input is the receive data serial input line, which carries RS-232 data.
C4-TXD	J004-c18	Transmit Data	This output is the transmit data serial output line, which carries RS-232 data.

8.2.7 Pinout of J003,J004 – Mass I/O – Floppy Disk Interface (J004)

For more information on Floppy Interface features, see section 6.14.

The Floppy feature is included in the basic board, requiring only the Mass I/O 5X22 (J004) connector to be ordered. For order information, see section 10.3.19.

Table 31 Signals – Mass I/O J003,J004 – Floppy Disk Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
F1-DENSL0#	J004-e20	Density Select	This signal Indicates whether a low (250/300 Kb/s) or high (500/1000 Kb/s) data rate has been selected.
F1-DIR#	J004-d21	Direction	This active low output determines the direction of the head movement (low = step-in, high = step-out). During the write or read modes, this output is high.
F1-DKCHG#	J004-a22	Disk Change	This disk interface input indicates when the disk drive door has been opened. This active-low signal is read from bit D7 of address xx7h.
F1-DS0#	J004-a20	Drive Select 0	Active low, output selects drive 0.
F1-DS1#	J004-b20	Drive Select 1	Active low, output selects drive 1.
F1-HDSEL#	J004-b22	Head Select	This active low output determines which disk drive head is active. Low = Head 0, high (open) = Head 1.
F1-INDEX#	J004-d20	Index Status	This active low Schmitt Trigger input signal senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
F1-MTR0#	J004-c20	Motor On 0	Active-low output selects motor drive 0.
F1-MTR1#	J004-e21	Motor On 1	Active-low output selects motor drive 1.
F1-RDATA#	J004-c22	Read Serial Data	This active-low, raw data read signal from the disk is connected here. Each falling edge represents a flux transition of the encoded data.
F1-STEP#	J004-c21	Step Head	This active low output signal produces a pulse at a software-programmable rate to move the head during a seek operation.
F1-TRK0#	J004-e22	Track 00	This active low Schmitt Trigger input signal senses from the disk drive that the head is positioned over the outermost track.
F1-WDATA#	J004-b21	Write Serial Data	This active low output is a write- precompensated serial data to be written onto the selected disk drive. Each falling edge causes a flux change on the media.
F1-WGATE#	J004-a21	Write Gate	This active-low, high-drive output enables the write circuitry of the selected disk drive. This signal prevents glitches during power-up and power-down. This prevents writing to the disk when power is cycled.
F1-WP#	J004-d22	Write Protected Status	This active-low Schmitt Trigger input signal senses from the disk drive that a disk is write-protected. Any write command is ignored.

8.2.8 Pinout of J003,J004 – Mass I/O – Panel Interface (J004)

For more information on Video features, see section 6.27.
For order information, see section 10.3.15.

Table 32 Signals – Mass I/O J003,J004 – Panel Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
L1-ACTI	J004-c7	Activity Indicator	(ACTI or A26 or GP0 or DDAT or CS) This signal is the Activity Indicator output. It may be configured for other functions (see Chips 65550 Datasheet – Extension Registers FR0C and FR0F and pin descriptions of MCD0-15 and A26/A27 for more information). I/O.
L1-ENABKL	J004-b7	Enable Backlight	(ENBKL or A27 or GP1 or DCLK or CS) This signal is the Enable Backlight output signal. It may be configured for other functions (see Chips 65550 Datasheet – Extension Registers FR0C and FR0F and pin descriptions of MCD0-15 and A26/A27 for more information). (Chips Revision 1.5 10/14/97 65550 Subject to Change without Notice). I/O.
L1-ENAVDD	J004-e7	Enable VDD	Power sequencing controls for panel driver electronics voltage VDD. I/O.
L1-ENAVEE	J004-a6	Enable VEE	(ENAVEE or ENABKL) Power sequencing controls for panel LCD bias voltage VEE, I/O. The polarity of this signal can be selected by option "d" - either active low or active high – see section 10.3.4.
L1-FLM	J004-b6	First Line Marker	Flat Panel equivalent of VSYNC. Active high. Output.
L1-FPD0	J004-e6	Data Output P0	Flat panel data output P0. Active high. Output.
L1-FPD1	J004-a5	Data Output P1	Flat panel data output P1. Active high. Output.
L1-FPD2	J004-b5	Data Output P2	Flat panel data output P2. Active high. Output.
L1-FPD3	J004-c5	Data Output P3	Flat panel data output P3. Active high. Output.
L1-FPD4	J004-d5	Data Output P4	Flat panel data output P4. Active high. Output.
L1-FPD5	J004-e5	Data Output P5	Flat panel data output P5. Active high. Output.
L1-FPD6	J004-a4	Data Output P6	Flat panel data output P6. Active high. Output.
L1-FPD7	J004-b4	Data Output P7	Flat panel data output P7. Active high. Output.
L1-FPD8	J004-c4	Data Output P8	Flat panel data output P8. Active high. Output.
L1-FPD9	J004-d4	Data Output P9	Flat panel data output P9. Active high. Output.
L1-FPD10	J004-e4	Data Output P10	Flat panel data output P10. Active high. Output.
L1-FPD11	J004-a3	Data Output P11	Flat panel data output P11. Active high. Output.
L1-FPD12	J004-b3	Data Output P12	Flat panel data output P12. Active high. Output.
L1-FPD13	J004-c3	Data Output P13	Flat panel data output P13. Active high. Output.
L1-FPD14	J004-d3	Data Output P14	Flat panel data output P14. Active high. Output.
L1-FPD15	J004-e3	Data Output P15	Flat panel data output P15. Active high. Output.
L1-FPD16	J004-a2	Data Output P16	Flat panel data output P16. Active high. Output.
L1-FPD17	J004-b2	Data Output P17	Flat panel data output P17. Active high. Output.
L1-FPD18	J004-c2	Data Output P18	Flat panel data output P18. Active high. Output.
L1-FPD19	J004-d2	Data Output P19	Flat panel data output P19. Active high. Output.

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
L1-FPD20	J004-e2	Data Output P20	Flat panel data output P20. Active high. Output.
L1-FPD21	J004-b1	Data Output P21	Flat panel data output P21. Active high. Output.
L1-FPD22	J004-d1	Data Output P22	Flat panel data output P22. Active high. Output.
L1-FPD23	J004-e1	Data Output P23	Flat panel data output P23. Active high. Output.
L1-LP	J004-c6	Latch Pulse	Flat Panel equivalent of HSYNC. Active high. Output.
L1-M	J004-d7	M signal	This signal is the M-signal for panel AC drive control (may also be called ACDCLK). May also be configured as BLANK# or as Display Enable (DE) for TFT Panels. Active High. Output.
L1-SHFCLK	J004-d6	Shift Clock	(SHFCLK or CL2 or SHFCLKL) This signal is the pixel clock for flat panel data. Active high. Output.

8.2.9 Pinout of J003,J004 – Mass I/O – Keyboard Interface (J004)

For information on Keyboard features, see section 6.15.
For order information for the Mass I/O 5X22 J004 connector, see section 10.3.19.

Table 33 Signals – Mass I/O J003,J004 – Keyboard Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
K1-CLK	J004-b8	Keyboard Clock	This output is the keyboard interface clock.
K1-DAT	J004-c8	Keyboard Data	This input is the keyboard serial data line.

8.2.10 Pinout of J003,J004 – Mass I/O – Mouse Interface (J004)

For information on Mouse features, see section 6.15.
For order information for the Mouse option, see section 10.3.12.
For order information for the Mass I/O 5X22 J004 connector, see section 10.3.19.

Table 34 Signals – Mass I/O J003,J004 – Mouse Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
M1-CLK	J004-d9	Mouse Clock	This output is the PS2 Mouse clock.
M1-DAT	J004-e9	Mouse Data	This input is the mouse serial data line.

8.2.11 Pinout of J003,J004 – Mass I/O – Reset Switch (J004)

For information about the Reset Switch feature, see section 6.21.

Table 35 Signals – Mass I/O J003,J004 – Reset Switch Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
MR-RSTSW#	J004-e8	Manual Reset	Hard Reset Input, Active low. This signal drives the Manual-Reset Input. An internal 40kΩ pull-up resistor (typical) is provided on this signal line. Leave open if unused. Reset remains asserted as long as this signal is held low and for 200ms (typical; minimum 140ms) after this signal is floated. **Normally there are two levels expected on this input line, an Active LOW level (-0.03V to +0.5V), and an Inactive HIGH level (Vcc-0.5V to Vcc+0.3V).** **However, for compatibility with the Megatel 104Family, Megatel strongly recommends that this input line should be tied to GROUND to activate the RESET function, and left OPEN otherwise. In any case, under no circumstances should this line be pulled higher than VCC3+0.3V (for the PC/II+dL, this limit is +3.6V).**

8.2.12 Pinout of J003,J004 – Mass I/O – Speaker (J004)

For information on use of the Speaker, see section 6.24.

Table 36 Signals – Mass I/O J003,J004 – PC Speaker Output Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
MS-SPKOUT	J004-a7	Speaker Output	This signal is used to control the Speaker Output and should connect to the Speaker.

8.2.13 Pinout of J003,J004 – Mass I/O – Parallel Printer Interface (J004)

For information on Parallel Port features, see section 6.18.

Table 37 Signals – Mass I/O J003,J004 – Parallel LPT1 Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
P1-AFD#	J004-b9	Autofeed Output	This active low output causes the printer to automatically feed one line after each line is printed. This signal is the complement of bit 1 of the Printer Control Register.
P1-AKN#	J004-e12	Acknowledge	This active low output from the printer indicates it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the PACK# input.
P1-BUSY	J004-d12	Busy	This signal indicates the status of the printer. A high indicates the printer is busy and not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input.
P1-D0	J004-a9	Port Data – Bit0	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D1	J004-d10	Port Data – Bit1	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D2	J004-b10	Port Data – Bit2	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D3	J004-e11	Port Data – Bit3	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D4	J004-d11	Port Data – Bit4	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D5	J004-c11	Port Data – Bit5	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D6	J004-b11	Port Data – Bit6	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D7	J004-a11	Port Data – Bit7	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-ERR#	J004-e10	Error	This active low signal indicates an error condition at the printer.
P1-INIT#	J004-c10	Initiate Output	This active low signal is bit 2 of the printer control register. This is used to initiate the printer when low.
P1-PE	J004-c12	Paper End	This signal indicates that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input.
P1-SLCT	J004-b12	Printer Selected Status	This active high output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input.
P1-SLIN#	J004-a10	Printer select input	This active low signal selects the printer. This is the complement of bit 3 of the Printer Control Register.
P1-STB#	J004-c9	Strobe Output	This active low pulse is used to strobe the printer data into the printer. This output signal is the complement of bit 0 of the Printer Control Register.

8.2.14 Pinout of J003,J004 – Mass I/O – SCSI (J004)

For information on SCSI I/O features, see section 6.22.
For order information on the SCSI option, see section 10.3.9.

Table 38 Signals – Mass I/O J003,J004 – SCSI Bus Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
S1-AKN#	J003-a8	Acknowledge	A signal driven by an initiator to indicate an acknowledgment for a REQ/ACK data transfer handshake.
S1-ATN#	J003-b8	Attention	A signal driven by an initiator to indicate the ATTENTION condition.
S1-BSY#	J003-e9	Busy	An "OR-tied" signal that indicates that the bus is being used. It may be driven by all SCSI devices that are actually arbitrating during Arbitration, driven by the initiator, target or both during Selection & Reselection, or driven by the target during all other phases.
S1-C/D#	J003-e8	Control/Data	A signal driven by a target that indicates whether CONTROL or DATA information is on the DATA BUS. True indicates CONTROL.
S1-D0#	J003-b9	Data Bus Bit Signal 0	Data bit signal 0. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. S1-D1# thru S1-D8# define eight data-bit signals. Together with the S1-DP# a parity-bit signal, they form a DATA BUS. S1-D7# is the most significant bit and has the highest priority during the ARBITRATION phase. Bit number, significance, and priority decrease downward to S1-D0#.
S1-D1#	J003-a9	Data Bus Bit Signal 1	Data bit signal 1. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-D2#	J003-e10	Data Bus Bit Signal 2	Data bit signal 2. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-D3#	J003-d10	Data Bus Bit Signal 3	Data bit signal 3. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-D4#	J003-c10	Data Bus Bit Signal 4	Data bit signal 4. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-D5#	J003-b10	Data Bus Bit Signal 5	Data bit signal 5. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-D6#	J003-a10	Data Bus Bit Signal 6	Data bit signal 6. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-D7#	J003-e11	Data Bus Bit Signal 7	Data bit signal 7. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
S1-DP#	J003-c9	Data Bus Parity	Data parity bit signal. Parity is Odd. Parity is undefined during the ARBITRATION phase. See S1-D0#.
S1-I/O#	J003-d8	Input/Output	A signal driven by a target that controls the direction of data movement on the DATA BUS with respect to an initiator. True indicates input to the initiator. This signal is also used to distinguish between SELECTION and RESELECTION phases.
S1-MSG#	J003-a7	Message	A signal driven by a target during the MESSAGE phase.
S1-REQ#	J003-b7	Request	A signal driven by a target to indicate a request for a REQ/ACK data transfer handshake.
S1-RST#	J003-c8	Reset	An "OR-tied" signal that indicates the RESET condition. The RST signal may be asserted by any SCSI device at any time.
S1-SEL#	J003-d9	Select	An "OR-tied" signal used by an initiator to select a target or by a target to reselect an initiator. NOTE: The SEL signal was not defined as "OR-tied" in SCSI-1. It has been defined as "OR-tied" in SCSI-2. This does not cause an operational problem in mixing SCSI-1 and SCSI-2 devices.

8.2.15 Pinout of J003,J004 – Mass I/O – Video CRT Interface (J004)

For information on Video features, see section 6.27.
For order information, see section 10.3.15.

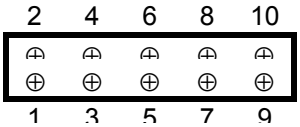
Table 39 Signals – Mass I/O J003,J004 – Video CRT Display Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
V1-B	J003-c1	CRT Blue	This Active High output signal is the BLUE CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm equivalent load on each pin (e.g. 75 ohm resistor on the board, in parallel with the 75 ohm CRT load).
V1-G	J003-d1	CRT Green	This Active High output signal is the GREEN CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm equivalent load on each pin (e.g. 75 ohm resistor on the board, in parallel with the 75 ohm CRT load).
V1-HSYNC	J003-b1	Horizontal Sync	(HSYNC or CSYNC) This Active High/Low output signal is the CRT Horizontal Sync (polarity is programmable) or the "Composite Sync" for support of various external NTSC/PAL encoder chips. Note CSYNC can be set to output on the L1-ACTI pin (Mass I/O pin J004-c7) or the L1-ENABKL pin (Mass I/O pin J004-b7).
V1-R	J003-e1	CRT Red	This Active High output signal is the RED CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm equivalent load on each pin (e.g. 75 ohm resistor on the board, in parallel with the 75 ohm CRT load).
V1-VSYNC	J003-a1	Vertical Sync	(VSYNC or VISINT) This Active High/Low output signal is the CRT Vertical Sync (polarity is programmable) or "VSync Interval" for support of various external NTSC/PAL encoder chips.

8.3 Pinout of J005 – Ethernet Connector

For information on Ethernet features, see section 6.9.
For order information for Ethernet, see section 10.3.5.

Figure 6 Diagram – Ethernet J005 – 2x5 Pin .100 Inch R/A Male Header



NOTES
[1] Top (component) view is shown.

8.3.1 Pinout – Ethernet

Table 40 Pinout – Ethernet J005 – 2x5 Pin .100 Inch R/A Male Header

PIN GROUP	PIN#	PIN NAME
E2-ETHERNET2 AUI	J005-1	**E2-CLSN-**
E2-ETHERNET2 AUI	J005-2	**E2-CLSN+**
E1-ETHERNET1 10BASE-T	J005-3	**E1-RD-**
E1-ETHERNET1 10BASE-T	J005-4	**E1-RD+**
E2-ETHERNET2 AUI	J005-5	**E2-RCV-**
E2-ETHERNET2 AUI	J005-6	**E2-RCV+**
E1-ETHERNET1 10BASE-T	J005-7	**E1-TD-**
E1-ETHERNET1 10BASE-T	J005-8	**E1-TD+**
E2-ETHERNET2 AUI	J005-9	**E2-TRMT-**
E2-ETHERNET2 AUI	J005-10	**E2-TRMT+**

Table 41 Signals – Ethernet J005 – 10Base-T Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
E1-TD-	J005-7	Negative Transmit Data	Negative Differential Manchester-encoded Transmit Data Line, 10 Mbps, from onboard 10 BASE T Isolation Transformer (1:SQRT(2)) Pin 11. Connect to external RJ45 connector Pin 2.
E1-TD+	J005-8	Positive Transmit Data	Positive Differential Manchester-encoded Transmit Data Line, 10 Mbps, from onboard 10 BASE T Isolation Transformer (1:SQRT(2)) Pin 9. Connect to external RJ45 connector Pin 1.
E1-RD-	J005-3	Negative Receive Data	Negative Differential Manchester-encoded Receive Data Line, 10 Mbps, to onboard 10 BASE T Isolation Transformer (1:1) Pin 16. Connect to external RJ45 connector Pin 6.
E1-RD+	J005-4	Positive Receive Data	Positive Differential Manchester-encoded Receive Data Line, 10 Mbps, to onboard 10 BASE T Isolation Transformer (1:1) Pin 14. Connect to external RJ45 connector Pin 3.

Table 42 Signals – Ethernet J005 – AUI Interface

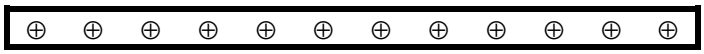
PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
E2-CLSN-	J005-1	Negative Collision In	Negative Differential AUI Collision Input Line, to onboard AUI Isolation Transformer Pin 13. Connect to external DB15 connector Pin 9.
E2-CLSN+	J005-2	Positive Collision In	Positive Differential AUI Collision Input Line, to onboard AUI Isolation Transformer Pin 10. Connect to external DB15 connector Pin 2.
E2-TRMT-	J005-9	Negative Transmit Data	Negative Differential Manchester-encoded Transmit Data Line, 10 Mbps, from onboard AUI Isolation Transformer Pin 16. Connect to external DB15 connector Pin 10.
E2-TRMT+	J005-10	Positive Transmit Data	Positive Differential Manchester-encoded Transmit Data Line, 10 Mbps, from onboard AUI Isolation Transformer Pin 15. Connect to external DB15 connector Pin 3.
E2-RCV-	J005-5	Negative Receive Data	Negative Differential Manchester-encoded Receive Data Line, 10 Mbps, to onboard AUI Isolation Transformer (1:1) Pin 10. Connect to external DB15 connector Pin 12.
E2-RCV+	J005-6	Positive Receive Data	Positive Differential Manchester-encoded Receive Data Line, 10 Mbps, to onboard AUI Isolation Transformer (1:1) Pin 9. Connect to external DB15 connector Pin 5.

8.4 Pinout of J007 – Power Connector (+5V)

For information on Power Arrangement features, see section 5, Electrical Specifications.
For order information for Power Supply Arrangement, see section 10.3.3.

Figure 7 Diagram – +5V Power Connector J007 – 1x12 PIN .100" R/A Male Header

1 2 3 4 5 6 7 8 9 10 11 12



NOTES
[1] Top (component) view is shown.

8.4.1 Pinout – +5V Power Connector

Table 43 Pinout – +5V Power Connector J007 – 1x12 PIN .100" R/A Male Header

PIN GROUP	PIN#	PIN NAME
POWER	J007-1	**+5V 5% from external supply**
POWER	J007-2	**+5V 5% from external supply**
POWER	J007-3	**+5V 5% from external supply**
POWER	J007-4	**KEY/GND**
POWER	J007-5	**GND**
POWER	J007-6	**GND**
POWER	J007-7	**GND**
POWER	J007-8	**GND**
POWER	J007-9	**GND**
POWER	J007-10	**+5V 5% from external supply**
POWER	J007-11	**+5V 5% from external supply**
POWER	J007-12	**+5V 5% from external supply**

8.5 Pinout of J008 – Fan Connector

This connector provides power only for an optional Cpu fan. The use of a Cpu fan is dependent upon the thermal operating environment for the PC/II+dL board, and is not normally required for systems using lower-speed processors.

The connector normally supplied on the PC/II+dL board is the MOLEX 53047-0210, a 1X2, 2mm pitch plug vertical connector.

For more information on Fan Connectors, see section 6.10.
For order information for the Fan connector, see section 10.3.2.

Table 44 Signals – Fan J008 – 1x2 1.25-mm Molex Connector

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
+5V	J008-a1	+5V	+5v
GND	J008-a2	GND	Ground

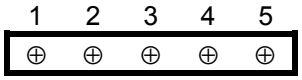
8.6 Pinout of J010 – Power Connector (+3.3V)

For information on Power Arrangement features, see section 5, Electrical Specifications.
For order information for Power Supply Arrangement, see section 10.3.3.

This connector is populated when the Dual Supplies option (Power Supply Arrangement) is ordered. All board +3.3v 5% power is supplied from an external source through this connector.

Note that when Single Supply option is ordered, J010 is not populated; instead, the board is shipped with an on-board +3.3v power supply.

Figure 8 Diagram – +3.3v Power Header J010 – 1x5 PIN .100" Male Header



NOTES
[1] Top (component) view is shown.

Table 45 Pinout – +3.3v Power J010 – 1x5 PIN .100" Male Header

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
+3.3V	J010-1	+3.3V	+3.3v 5% from external supply
GND/KEY	J010-2	GND/KEY	Ground (or Key)
GND	J010-3	GND	Ground
GND	J010-4	GND	Ground
+3.3V	J010-5	+3.3V	+3.3v 5% from external supply

9 Peripheral Attachment (QTB/dxp)

PC/II+dL and other megatel 104Family Cpu boards can be attached to peripherals by user-supplied cabling that mates directly with the on-board Mass I/O Connector and/or Ethernet Header. Megatel also provides an economical transition board set for this family of boards. The transition cards are compatible electrically with prior QTB boards, and pull all Cpu board signals to industry-standard connectors and headers.

Refer to the Megatel document, QTB/Dxp Technical Reference Manual, document MT002110a, for detailed specifications. You can obtain this a copy of this PDF-format document on the Megatel web site, http://www.megatel.ca.

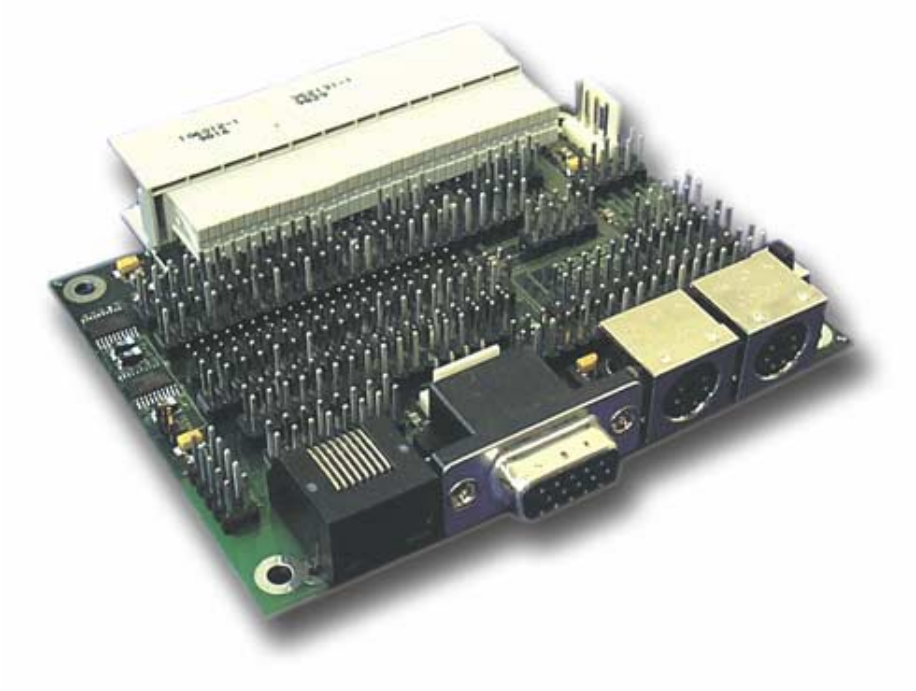


Figure 9 QTB/Dxp I/O Transition Board (v2.10)

The QTB/dxp transition board mates side-by-side with the PC/II+dL, to both the PC/II+dL Mass I/O connectors, and via optional cable to the PC/II+dL Ethernet header. The PC/II+dL in this configuration uses the AMP Z-PACK right-angle receptacle (female) connectors for both J003 and J004; the QTB/dxp uses the plug (male) versions.

The QTB/dxp board is approximately 3.775 by 2.95 inches, and mates to the PC/II+dL on the long side. It is supplied by two power

Connectors provided on the QTB/dxp board include the following:

- ✓ Cpu board interface connectors
- ✓ Power
- ✓ Serial – 4 ports
- ✓ Parallel port
- ✓ LCD
- ✓ VGA
- ✓ Keyboard & Mouse
- ✓ Ethernet AUI
- ✓ Ethernet 10Base-T
- ✓ SCSI 26-pin and 50-pin
- ✓ IDE 40-pin (.100) and 44-pin (2mm)
- ✓ Floppy
- ✓ USB (unused)
- ✓ Miscellaneous

The QTB/dxp also contains an active termination circuit for the SCSI bus, using Dallas Semiconductor DS2107 active terminators. Jumper JP01 on the circuit board can be installed to remove the active terminator from the host end of the SCSI bus. This would be used to insert the host into the middle of the SCSI bus. Without the jumper installed, the host termination is active.

The following table summarizes the connectors and headers available on a QTB/dxp transition board. To obtain detailed information concerning the QTB/dxp board, please refer to the megatel QTB/dxp Technical Reference documentation.

Table 46 QTB/dxp Connector List

Ref	Connector / Header Description
J901	Mass I/O Board Connector – 5x22 AMP Z-PACK 2mm HM Right-angle plug (male)
J902	Mass I/O Board Connector – 5x11 AMP Z-PACK 2mm HM Right-angle plug (male)
J003	4-Pin System Power (+5v, Gnd, Gnd, N/C)
J004	COM1 Header – 10-pin 2x5 (0.100" pitch) Header
J005	COM2 Header – 10-pin 2x5 (0.100" pitch) Header
J006	COM3 Header – 10-pin 2x5 (0.100" pitch) Header
J007	COM4 Header – 10-pin 2x5 (0.100" pitch) Header
J008	LPT1 Parallel Port (Printer) Header – 26-Pin 2x13 (0.100" pitch) Header
J009	LCD Header – 36-pin 2x18 (0.100" pitch) Header
J010	Reset Switch – 3-Pin Standard Straight-Up or 4-pin Right-angle SPST Momentary Switch
J011	Keyboard Connector – MiniDIN6 PS/2-style Keyboard Connector (mounted at edge of card)
J012	Mouse Connector – MiniDIN6 PS/2-style Mouse Connector (mounted at edge of card)
J013	Miscellaneous Header – 6-pin 1x6 (2mm pitch) Header
J014	VGA Monitor Connector – DE15 Female (mounted at edge of card)
J015	Ethernet AUI Power Connector – 4-pin (+12v,Gnd,Gnd,N/C)
J016	Ethernet AUI Header – 16-pin 2x8 (0.100" pitch) Header
J017	Ethernet 10Base-T Connector – RJ-45 Connector (mounted at edge of card)
J018	Ethernet Board Header – 10-pin 2x5 (0.100" pitch) Header
J020	SCSI Header – 50-pin 2x25 (0.100" pitch) Header
J021	IDE/ATA Header – 40-pin 2x20 (0.100" pitch) Header
J022	IDE/ATA Header – 44-pin 2x22 (2mm pitch) Header
J023	Floppy Connector – 34-pin 2x17 (0.100" pitch) Header
J024	USB Header
J025	Reset Switch – 4-pin Right-angle SPST Momentary Switch
J026	USB Connector – Dual Stacking
J027	Speaker Header – 2-pin (0.100" pitch) Speaker-Output Header
JP01	SCSI Terminator Jumper – Enable (Shunt Present) or Disable (Shunt Removed)

10 Order Information

The PC/II+dx may be ordered directly from Megatel or through one of our representatives.

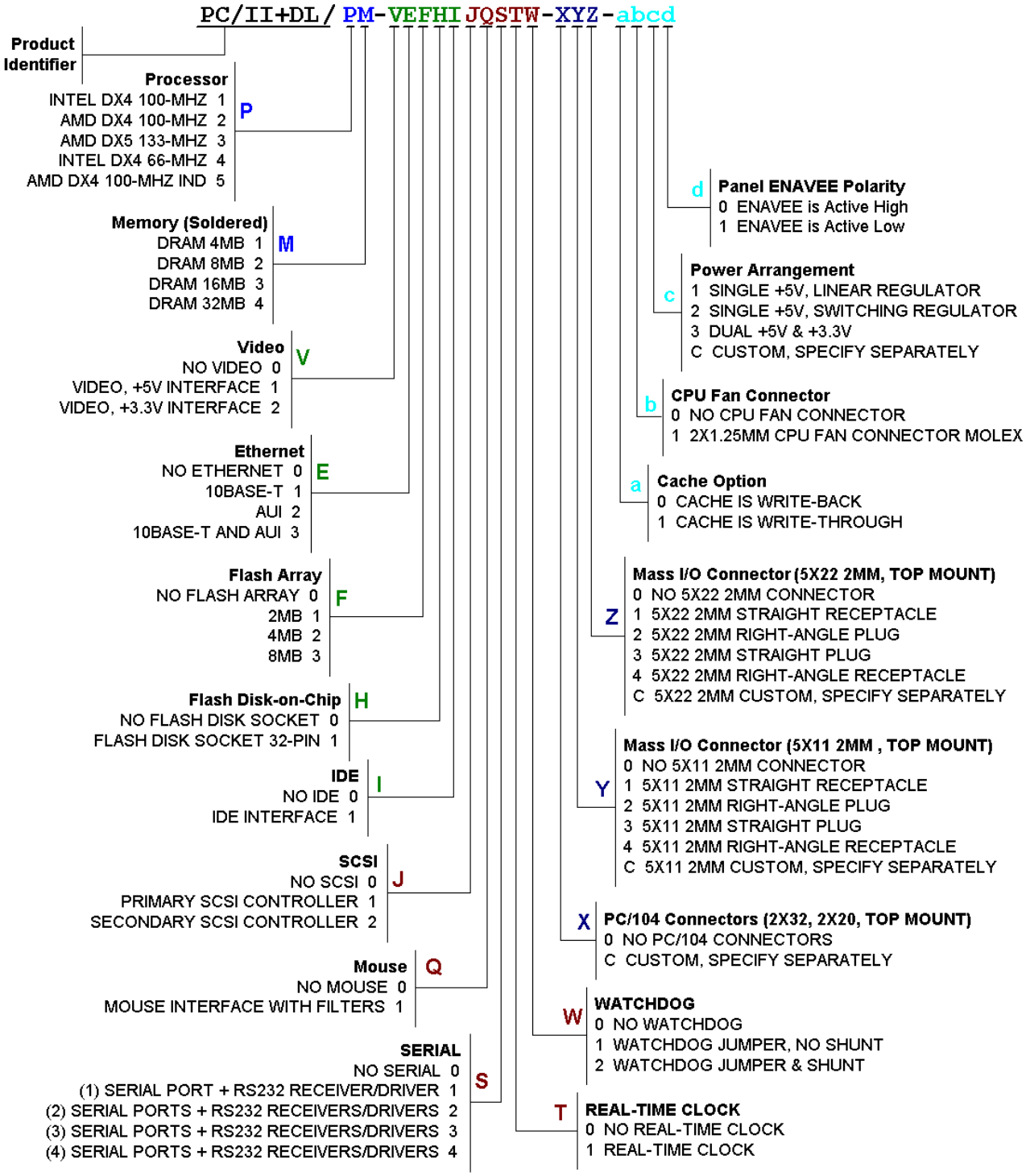
To provide an off-the-shelf solution that can be tailored to exactly match your requirements in the smallest most cost-effective package possible, manufacturing and design work is performed in-house, and products have been designed to be populated with a variety of optional components, which you can choose by selecting the corresponding model number for the product.

First time buyers might opt to purchase one of our OEM development kits which includes all the necessary items to get started quickly.

Small quantity orders (1–4) are normally available within 2 weeks. For larger orders, please allow 4 to 6 weeks for delivery.

10.1 PC/II+dL Product Numbering

You can use the generic model number below to select your model number, or use the calculator on Megatel's website, http://www.megatel.ca, to help you.



10.2 PC/C/II+dL Specific Order Example

Example :

	Processor	Memory		Video	Ethernet	Flash Array	Flash Disk-on-Chip Socket	IDE	SCSI	Mouse	Serial I/O	Real-Time Clock & Battery	Watchdog		PC/104	MASS I/O 5X11	MASS I/O 5X22		Cache Bus Protocol	Fan Connector	Power Supply Arrangement	Panel ENAVEE Polarity
PC/II+dL/	**P**	**M**	**-**	**V**	**E**	**F**	**H**	**I**	**J**	**Q**	**S**	**T**	**W**	**-**	**X**	**Y**	**Z**	**-**	**a**	**b**	**c**	**d**
PC/II+dL/	**4**	**1**	**-**	**2**	**1**	**3**	**1**	**1**	**0**	**1**	**4**	**1**	**2**	**-**	**0**	**4**	**4**	**-**	**1**	**0**	**3**	**0**

P=4 INTEL DX4 66 MHz Processor
M=1 4 MB Soldered DRAM
V=2 Video (with 2 MB Video DRAM) and +3.3V panel interface
E=1 Ethernet 10Base-T interface (with Isolation Transformer)
F=3 8 MB Flash Array Soldered
H=1 Flash Disk Socket
I=1 IDE Interface (2 Drives)
J=0 SCSI Bus Interface (7 Drives)
Q=1 Mouse
S=4 4 Serial 16550 RS-232 Channels (Including Transceivers)
T=1 Real-Time Clock with Battery Backup installed
W=2 Watchdog Jumper & Shunt installed
X=0 PC/104 connectors not installed
Y=4 Mass I/O 5X11 IEC 2mm HM Right-Angle Receptacle Connector installed
Z=4 Mass I/O 5X22 IEC 2mm HM Right-Angle Receptacle Connector installed
a=1 Cache uses Write-Back protocol (faster)
b=0 Fan connector not installed
c=3 Power Arrangement = "Dual Supplies": both +5V and +3.3V supplied to board
d=0 Panel ENAVEE is Active High

10.3 PC/II+dL Order Options

Order options are listed in the following sub-sections, in alphabetical order of OPTION LETTER. Use the order option code for each order option to form the product model number that is used to order boards – see section 10.1 for the product order numbering rules.

The following options are given below:

Option a	Section 10.3.1	*Cache Memory (L1) Bus Protocol*
Option b	Section 10.3.2	*Fan Connector*
Option c	Section 10.3.3	*Power Supply Arrangement*
Option d	Section 10.3.4	*Panel ENAVEE Polarity*
Option E	Section 10.3.5	*Ethernet*
Option F	Section 10.3.6	*Flash Array*
Option H	Section 10.3.7	*Flash Disk-on-Chip Socket*
Option I	Section 10.3.8	*IDE*
Option J	Section 10.3.9	*SCSI*
Option M	Section 10.3.10	*Memory*
Option P	Section 10.3.11	*Processor*
Option Q	Section 10.3.12	*Mouse*
Option S	Section 10.3.13	*Serial*
Option T	Section 10.3.14	*Real-Time Clock & Battery*
Option V	Section 10.3.15	*Video*
Option W	Section 10.3.16	*Watchdog*
Option X	Section 10.3.17	*PC/104*
Option Y	Section 10.3.18	*Mass I/O 5X11*
Option Z	Section 10.3.19	*Mass I/O 5X22*

10.3.1 Option a – CACHE Memory (L1) Bus Protocol Option

0	Cache (L1) operates in WRITE-BACK mode
1	Cache (L1) operates in WRITE-THROUGH mode

NOTES.
See section 6.6 for a more complete description of when to use either Caching option.
Please contact your Representative or contact Megatel engineering for more information.

10.3.2 Option b – Fan (5v) Connector (J008)

0	NONE
1	FAN Connector J008 (5v- Molex type – 1.25-mm pitch)
C	Custom 1x2 1.25-MM Pitch Connector

NOTES.
Air flow is recommended with a processor operating above 66 MHz.
Contact your Representative or Megatel engineering to verify your environmental requirements.
See section 6.10 for more information about the Fan Connector.

10.3.3 Option c – Power Supply Arrangement

1	SINGLE LINEAR Single +5v 5% Supply Required to Power Board. Connector J007 (12-pin header) supplies +5v. LINEAR P.S. (on-board) supplies +3.3v.
2	SINGLE SWITCHING Single +5v 5% Supply Required to Power Board. Connector J007 (12-pin header) supplies +5v. SWITCHING P.S. (on-board) supplies +3.3v.
3	DUAL SUPPLIES Dual +5v 5% and +3.3v 5% Required to Power Board. Connector J007 (12-pin header) supplies +5v. Connector J010 (5-pin header) supplies +3.3v.
C	Power Supply Arrangement is CUSTOM

NOTES.
J007 (+5V Power Header) is always populated.
J010 (+3.3V Power Header) is populated only when option 3 is selected
For option 3, the on-board power supplies are not populated, since power is externally sourced.
See section 5 for more information about electrical requirements.

10.3.4 Option d – Panel ENAVEE Polarity

0	ENAVEE is Active High
1	ENAVEE is Active Low

NOTES.
See section 6.27 for more information about Video features.
See section 8.2.8 for panel interface pinouts.

10.3.5 Option E – Ethernet

0	NONE
1	Ethernet 10BASE-T with Filters & Transformer, and Header (J005)
2	Ethernet AUI with Filters & Transformer, and Header (J005)
3	Ethernet 10BASE-T & AUI with Filters & Transformers, and Header (J005)

NOTES.
J005 (Ethernet Header) is populated when option 1, 2, or 3 is ordered.
See section 6.9 for more information on Ethernet features.
See section 8.3 for Ethernet pinout information.

10.3.6 Option F – Flash Array

0	NONE
1	2MB User Flash Array, soldered
2	4MB User Flash Array, soldered
3	8MB User Flash Array, soldered

NOTES.
See section 6.12 for more information on Flash Array features.

10.3.7 Option H – Flash Disk-on-Chip Socket

0	NONE
1	Flash Disk Socket for User-supplied SSD module (such as M-Systems' Disk-on-Chip® module

NOTES.
See section 6.13 for more information on Flash Disk features.

10.3.8 Option I – IDE Bus Interface

0	NONE
1	IDE Bus, provided on Mass I/O 5X11 Connector (J003)

NOTES.
Requires Mass I/O 5X11 connector (J003) to be present. See section 10.3.18 (order option "Y").
See section 6.25 for more information on IDE features.
See section 8.2.2 for IDE pinout information.

10.3.9 Option J – SCSI Bus

0	NONE
1	Primary SCSI Controller; Termination is provided off-board. SCSI is configured as Primary Controller (base I/O address 340h).
2	Secondary SCSI Controller; Termination is provided off-board. SCSI is configured as Secondary Controller (base I/O address 140h).

NOTES.
Requires Mass I/O 5X11 connector (J003) to be present. See section 10.3.18 (order option "Y").
See section 6.22 for more information on SCSI features.
See section 8.2.14 for SCSI interface pinout information.

10.3.10 Option M – Memory

1	4 MB Soldered EDO DRAM
2	8 MB Soldered EDO DRAM
3	16 MB Soldered EDO DRAM
4	32 MB Soldered EDO DRAM

NOTES.
See section 6.16 for more information on Memory features.

10.3.11 Option P – Processor

1	INTEL DX4 100 MHz Processor, Soldered
2	AMD DX4 100 MHz Processor, Soldered
3	AMD DX5 133 MHz Processor, Soldered
4	INTEL DX4 66 MHz Processor, Soldered
5	AMD DX4 100 MHz Industrial Processor, Soldered

NOTES.
To determine the latest processor options that are available, please contact your representative or Megatel.
Air flow is recommended with a processor operating above 66 MHz.
See section 10.3.2 (order option "b" – Fan connector).
See section 6.4 for more information about processor options.

10.3.12 Option Q – Mouse

0	NONE
1	Mouse Interface (with Filters), provided on Mass I/O 5X22 connector (J004)

NOTES.
Requires Mass I/O 5X22 connector (J004) to be present, see section 10.3.19 (order option "Z").
See section 6.15 for more information on Mouse interface.
See section 8.2.10 for Mouse interface pinout information.

10.3.13 Option S – Serial Ports

0	NONE
1	COM1 (1) 16550 Serial Port, provided on Mass I/O 5X22 (J004)
2	COM1, COM2 (2) 16550 Serial Ports, provided on Mass I/O 5X22 (J004)
3	COM1, COM2, COM4 (3) 16550 Serial Ports, provided on Mass I/O 5X22 (J004)
4	COM1, COM2, COM3, COM4 (4) 16550 Serial Ports, provided on Mass I/O 5X22 (J004)

NOTES.
Requires Mass I/O 5X22 connector (J004) to be present. See section 10.3.19 (order option "Z").
Each installed serial port contains a 16550-compatible UART (with FIFOs).
Each installed serial port contains all required RS-232 driver and receivers for the I/O interface lines.
See section 6.23 for more information on Serial Port features.
See sections 8.2.3, 8.2.4, 8.2.5 and 8.2.6 for Serial Port pinout information.

10.3.14 Option T – Real-Time Clock

0	NONE
1	Real-Time Clock with Battery Backup is installed

NOTES.
The Real Time Clock's RAM holds BIOS system configuration data; when the Real-Time clock is not installed, this configuration data is hard-coded into the BIOS for the user. Contact Megatel Engineering for details on how to order hard-coded BIOS configuration.
See section 6.20 for more information about Real-Time clock features.
See section 6.20.2 for Lithium Battery information.

10.3.15 Option V – Video

0	NONE
1	Video with +5V Panel/CRT Interface and 2MB Fast EDO Video Memory.
2	Video with +3.3V Panel/CRT Interface and 2MB Fast EDO Video Memory.

NOTES.
Requires Mass I/O 5X22 connector (J004) to be present. See section 10.3.19 (order option "Z").
See section 6.27 for more information on Video features.
See sections 8.2.8 and 8.2.15 for Video Panel and CRT pinout information, respectively.

10.3.16 Option W – Watchdog

0	NONE Watchdog jumper is not Installed – Watchdog is disabled on the shipped board. It cannot be enabled.
1	Watchdog JUMPER INSTALLED, NO SHUNT No Shunt – as shipped, the Watchdog acts as in option "0". Shunt – a shunt can be user-inserted into JP01; in this case the Watchdog acts as in option "2".
2	Watchdog JUMPER AND SHUNT INSTALLED The Watchdog jumper and shunt are both Installed on the shipped board. The BIOS automatically deactivates the Watchdog at system boot time. An application can Activate the Watchdog using the BIOS Watchdog programming interface.

NOTES.
See section 6.28 for more information on Watchdog features.

10.3.17 Option X – PC/104

0	NONE
C	PC/104-AB (2X32,.100 INCH) AND PC/104-CD (2X20,.100 INCH) CONNECTORS ARE CUSTOM

NOTES.
See section 8.1 for PC/104 connector pinout information.

10.3.18 Option Y – MASS I/O 5X11 (J003)

0	NONE
1	Mass I/O 5X11 (J003) Straight Receptacle – AMP Z-PACK IEC 2MM HM
2	Mass I/O 5X11 (J003) Right Angle Plug – AMP Z-PACK IEC 2MM HM
3	Mass I/O 5X11 (J003) Straight Plug – AMP Z-PACK IEC 2MM HM
4	Mass I/O 5X11 (J003) Right Angle Receptacle – AMP Z-PACK IEC 2MM HM
C	Mass I/O 5X11 (J003) CUSTOM

NOTES.
Mass I/O J003 and J004 connectors are required if any peripheral function except for Ethernet is required.
See section 8.2 for a complete list of peripheral groups that require this option.

10.3.19 Option Z – MASS I/O 5X22 (J004)

0	NONE
1	Mass I/O 5X22 (J004) Straight Receptacle – AMP Z-PACK IEC 2MM HM or equivalent
2	Mass I/O 5X22 (J004) Right Angle Plug – AMP Z-PACK IEC 2MM HM or equivalent
3	Mass I/O 5X22 (J004) Straight Plug – AMP Z-PACK IEC 2MM HM or equivalent
4	Mass I/O 5X22 (J004) Right Angle Receptacle – AMP Z-PACK IEC 2MM HM or equivalent
C	Mass I/O 5X22 (J004) CUSTOM

NOTES.
Mass I/O J003 and J004 connectors are required if any peripheral function except for Ethernet is required. See section 8.2 for a complete list of peripheral groups that require this option.

11 Service Information

If you feel your board requires service, Megatel Service Department will do all it can to get you up and running – quickly.

If you purchased your board from a Distributor:

Our distributors are technically capable and will help you to determine and correct your problem. Since your proof of purchase was obtained from the Distributor, please return your board to them. Please follow their instructions for returning your board for service.

If you purchased your board directly from Megatel:

Please Call or Fax to Megatel's Service Department prior to shipping, to receive your RMA# (Return Materials Authorization number). You may also submit a request for an RMA# from our web-site http://www.metatel.ca. Boards that do not have RMA#s will not receive priority. To receive an RMA#, you will be required to provide the following information:

1. Company Name
2. Board Model Number or Product Order Number
3. Board Serial Number
4. Description of the Problem
5. Purchase Order Number

Special Shipping Instructions

Along with the information on the Megatel SERVICE FORM (see next page), please include the following on one of your commercial invoices:

1. The value of the board(s) – this value must match the invoice(s) we sent with the boards
2. A copy of the invoice(s) we sent with the boards (Proof of Purchase)
3. Be sure to state one of the following
   a) "Canadian Goods Being Returned for Repair"
   b) "Canadian Goods Being Returned for Warranty Repair"
   c) "Canadian Goods Being Returned"

One copy of the above documents is to be placed inside the shipping box and one copy is to be placed on the outside of the shipping box (marked for CUSTOMS). Other products (i.e. disk drives, LCD panels, etc.) that were not purchased from Megatel, but will be used as part of the servicing of the returned board, must be shipped separately and listed in the Megatel SERVICE FORM (next page) under "Equipment Sent Separately" heading. Products not purchased from Megatel should be shipped under a temporary import license of the maximum time limit.

Send PREPAID to the SERVICE DEPT. at:

MEGATEL COMPUTER CORPORATION
125 WENDELL AVENUE
WESTON, ONTARIO
M9N 3K9 CANADA

Our harmonized Number: 8471.92.00

Call us at +1 416 245-2953 between 9:00 am to 5:00 pm EST or send a Fax to +1 416 245-6505.

Megatel SERVICE FORM

PRIOR TO SHIPPING: : Please call Megatel to receive your RMA#. Only boards sent with an RMA# will be given priority. This RMA# must appear on all paper work and be clearly marked on the outside of the shipping box.

RMA#: _____

Date Called: _____

Your Company Name: _____

Your Contact Name: _____

Your Company Address:

Ship To: _____ **Bill To:** _____

Your Telephone Number: _____ **Extension:** _____

Your Fax Number: _____ **Extension:** _____

Equipment You are Sending to Us: Pleasefill in the following as completely and accurately as possible

Product #	Serial #	Description of the Problem

Purchase Order Number for this Return _____

Equipment Sent Separately

Courier	Waybill#	Description (include Model#, Serial#)

Courier Company to be Used for Returning this Shipment: Please Circle or Check One

FEDEX	EMERY	UPS AIR	PUROLATOR	ALPHA	TRANS	BAISLEY

OTHER _____

Special Instructions/Comments You have for us: _____

12 Physical Specifications

The physical size of the PC/II+dL is compliant with the PC/104 Specification. The size is 3.775 x 3.550 inches (95.9 x 90.2 mm). In the diagram, connectors J1 and J2 are specified by the PC/104 specification, and J3, J4, J5 and J7 are the megatel Mass I/O 5X11 connector, Mass I/O 5X22 connector, Ethernet Header and Power Connector, respectively.

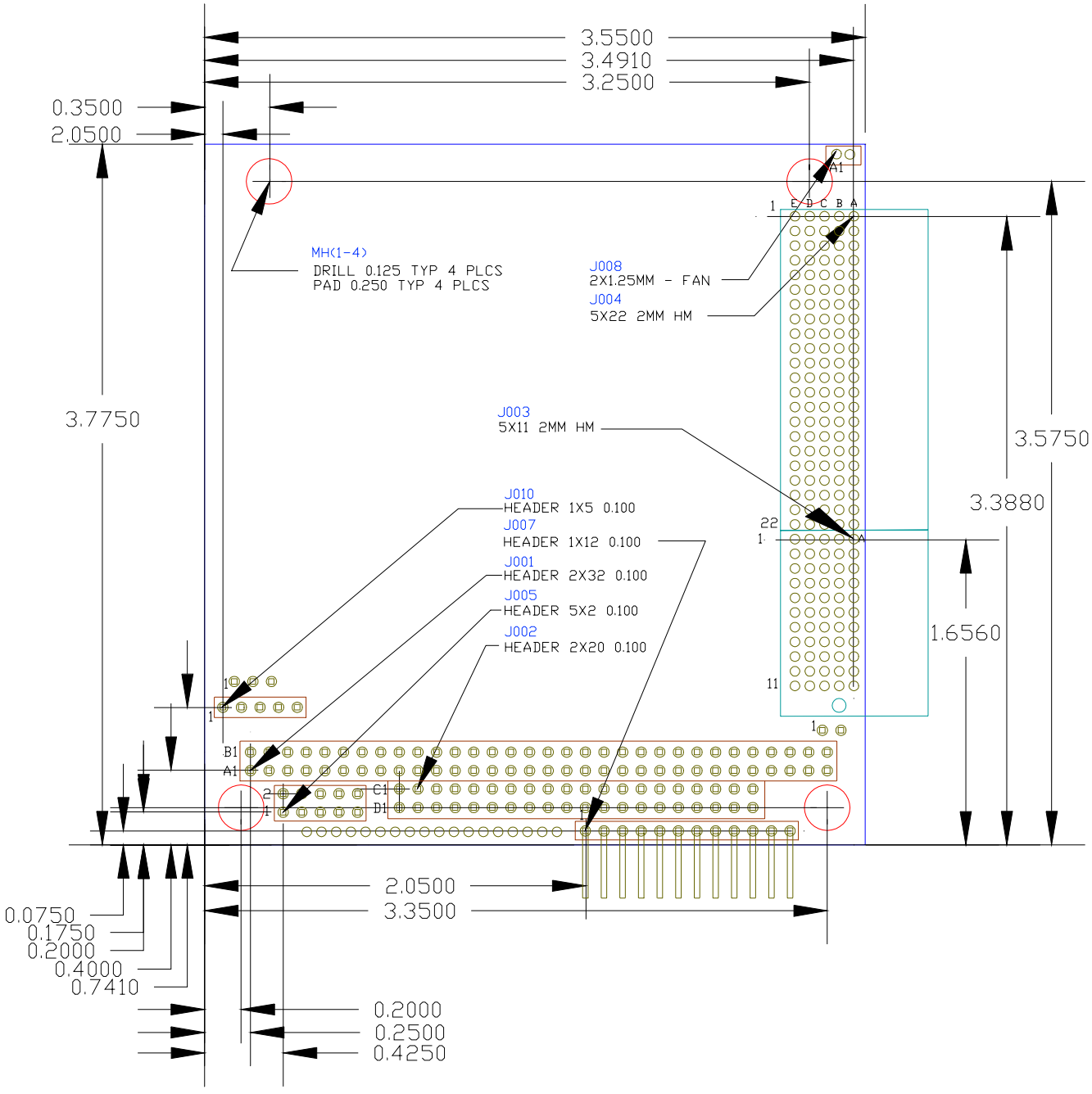


Figure 10 PC/II+dL Physical Dimensions (v1.03)

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