megatel

PC/II+vxe

Low Cost Single-Board Embedded Computer

Technical Reference Manual

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PC/II+vxe

Low-Power Single-Board Embedded Computer

megatel

4x4Family

Product Brief

The **PC/II+vxe** is a rugged single-board computer with a wide range of features that made us famous. This board is compliant to the Megatel 4x4Family mechanical and pin specification. PC/104 connectivity is also available. And it is available with a broad set of options that can be mixed in any combination to maximize price and performance.

The PC/II+vxe board features a x86-compatible 8/bit 20 MHz processor (V40™), a National PC97307 Super I/O, an Intel/Chips 65550 Video controller for SVGA CRT and 8- to 24-bit flat panels, and a SCSI controller with optional Active Terminator. The board uses a 256KB BIOS flash, offers a user Flash Array of 2 to 8MB in size, and offers a Disk-on-Chip 32-pin DIP socket for user population of up to 144+ MB of flash disk. Many other standard peripheral options are available.

The PC/II+vxe PCB is manufactured on FR4 with all parts mounted on the top (component) side of the board (excluding the optional X-32 socket).

We think you'll agree that the outstanding features, ruggedness, low power and low price all combine to make this, the board of choice for upgrading your applications and for new design-ins.

Features

- **Megatel PC/II+vxe Board with x86-compatible 20 MHz Processor (NEC V40HL™)**
- **640 KB main memory (EDO DRAM)**
- **Altera PLD**
- **128 KB or 256 KB BIOS Flash**
- **National PC97307 Super I/O**
- **PS/2 & Optional PS/2 Mouse, or XT compatible Keyboard interface**
- **Floppy Disk Controller – for up to 2 Drives**
- **Megatel 4x4Family-compatible 96-pin I/O Interface uses Eurocard (DIN) Connector System**
- **Power Monitor & Optional Watchdog**
- **Optional Flash Array – 2MB, 4MB or 8MB of soldered flash**
- **Optional Flash Disk – 32-pin DIP socket for user Disk-on-Chip, 2-144MB**
- **Optional Intel/Chips 65550 CRT/Panel Controller (SVGA/8/16/24-bit Panels) with 2 MB Video EDO DRAM**
- **Support for both +5V and +3.3V Panels**
- **Optional SCSI Controller**
- **Two Optional Full 16550 RS-232 Serial Ports**
- **One Optional 2-wire RS-232 Serial Port**
- **Optional SPP Parallel Port**
- **Optional RTC (Y2K) provided by PC97307**
- **Optional PC® ISA Bus Support (and PC/104 connectivity)**

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There were no significant changes made to v1.16 of the PCB	
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There were no significant changes made to v1.17 of the PCB.	
This PCB was updated to change the package a small logic IC (bus switch part)	
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Release Version for PC/II+vxe v1.18

Production Release of PCB - no significant changes were made to v1.18 of the PCB

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Release Version for PC/II+vxe v1.19

Production Release of PCB - no significant changes were made to v1.19 of the PCB	
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1 Introduction

We would like to introduce you to the Megatel PC/II+vxe Cpu board, one of the Megatel 4x4Family Cpu boards from Megatel Computer Corporation. In this document, you will find specifications for the functional, electrical, physical and operating characteristics of the PC/II+vxe Cpu board. Please feel free to contact Megatel or one of its distributors or agents if you require more information.

We have organized this document to present reference material, quick specifications, board settings and electrical specifications. The functional specifications begin in Functional Specifications, in topical order, including an introductory parts list and component placement diagrams. We conclude this document with resource maps, connector pinouts and signals, ordering and servicing information. Physical board specifications are placed at the end of the document.

1.1 PC/II+vxe Overview

PC/II+vxe is Megatel 4x4Family compliant in its form factor and electrical interfaces. As a member of the Megatel 4x4Family, it is interchangeable with other members of the family to provide the feature set and performance range you require. The PC/II+vxe provides an 8-bit PC® ISA bus interface connector (J902) and a 96-pin Eurocard (DIN) I/O connector (J901) to allow direct drop-in compatibility with existing and new designs.

PC/II+vxe contains a 20 MHz x86-compatible (V40HL™) processor, 640 KB of main memory (2 MB of EDO DRAM are on-board), an on-board Altera CPLD, a 128 KB or 256 KB BIOS flash memory, and a National PC97307 Super I/O controller to provide support for standard PC® peripherals. It also optionally contains an Intel/Chips 65550 SVGA CRT/panel controller with support for SVGA CRT peripherals and a variety of flat panels, both the 8-/12-bit 4x4Family compatible panel interface and a full 24-bit panel interface, 2MB of EDO DRAM Video Memory, a SCSI controller and SCSI bus interface with optional Active SCSI Terminator, a soldered user Flash Array (2MB to 8MB), and a Disk-on-Chip 32-pin DIP socket for user population of an additional 2MB to 144MB of flash disk space.

PC/II+vxe is manufactured on FR4, and excluding the optional flash disk socket, all parts are top-mounted. The board contains a Eurocard DIN 96-pin peripheral I/O connector (or any other header/connector that can be populated on a .100 inch 3x32 through-hole grid), an optional 8-bit PC® ISA bus header (or other headers/connectors that can be populated on a .100 inch 2x32 through-hole grid), and an optional 24-bit panel header (or any other header that can be populated on a 2x18 .100 inch through-hole grid). A single +5V supply is required to be supplied using the power pins on the 96-pin DIN connector (J901); a small 3.3V supply requirement is generated by the on-board regulator. Alternatively, both +5V and +3.3V can be supplied externally to the board. The board measures 100 mm x 100 mm (4” by 4”).

A rich complement of peripheral support interfaces is included. The full video interface supports SVGA CRT (R, G, B, Hsync, Vsync) and/or a wide variety of 8-bit, 16-bit or 24-Bit flat 5V or 3.3V panels. The SCSI interface supports a fast SCSI-2 bus interface. And interfaces are also provided on-board for a PS/2-style (or XT-style) Keyboard, a PS/2-style mouse, 2-drive Floppy bus, a full SPP parallel port, two standard RS-232 serial ports, and a two-wire BIOS-supported RS-232 channel. Peripheral I/O is pulled to the 96-pin DIN connector (J901), an optional 2-pin PS/2 Mouse header, and an optional 36-pin 24-bit Video Panel header.

The Megatel 4x4Family PC/II+vxe has been designed for rugged and reliable operation in a low-cost compatible package, and extends the Megatel 4x4Family product line. ***Any combination*** of peripherals can be ordered and will be populated specifically to meet your price/performance requirements. We think you'll agree that the outstanding features, low power and low price all combine to make this, the board of choice for upgrading your applications and for new design-ins.

2 Reference Documents

2.1 Datasheets

Adaptec	AIC-6360 Data Book PC-AT to SCSI Host Adapter,
Analog Devices	EMI/EMC Compliant ±15 kV ESD Protected RS-232 Line Drivers/Receivers (ADM211E), 1996
Intel (Chips and Tech)	65550 (HiQV32™) High Performance Multi-Media Flat Panel / CRT GUI Accelerator, Revision 1.5, Dec 1997 65550 HiQVideo Series Mode Support, 020089-004 (AN89.4), Revision 1.4, Feb 1996
Dallas Semiconductor	DS1706S 3.3V and 5.0V MicroMonitor, Feb 1998 DS21S07A SCSI Terminator, 022798
Intel	INTEL® StrataFlash™ Memory Technology 32 and 64 Mbits (28F640J5), 290606-006, Jul 1998
National	PC97307 Plug and Play Compatible PC97 Compliant Super I/O, March 1996
NEC	uPD70208 V40HL™, Document U13225EJ3V0DS00 (3Rd Edition, March 1998) V-Series (V40HL™) Preliminary User's Manual, Volume 1 and Volume , IEU-770B-V1 and IEU-770B-V2, 1993

2.2 Reference Standards

Annabooks	AT Bus Design IEEE P996-Compatible, Edward Solari
IEEE	P996.1 Standard for Compact Embedded-PC Modules

2.3 Other References

Microsoft Press	The Programmer's PC Sourcebook, Thom Hogan

3 Specification Summary

3.1 PC/II+vxe Board Specifications

Board Form Factor: 3.937 x 3.937 inch (100.0 x 100.0 mm)
Board Type: FR4
Basic Board Requires: Central Processing Unit
Main Memory 640 KB EDO DRAM
Minimum Connectors – 96-pin DIN connector (J901)

Architecture: PC® / XT
Central Processing Unit: x86-Compatible Processor (V40HL™/188)
V40HL™:
- 20 MHz core speed (100 ns execution time)
- Zero wait-state 20 MHz local bus for on-board memory & I/O
- 5V high-speed, low power
- 16-/8-bit architecture/data bus
- Memory Refresh controller
- Timer/counter controller
- Serial controller
- Interrupt controller
- DMA controller

DMA: (3) Channels
- 1 MB (20-bit) addressable
- 16-bit transfer counters

Interrupts: (8) Interrupt levels
- (7) external interrupt sources, (1) internal
- Edge/level triggered (TCU is edge only)
- All inputs individually maskable
- All inputs priority programmable
- Polling capable

Timer/Counters: (3) 16-bit timers/counters
- (6) programmable counter modes
- binary/BCD
- multiple latch
- clock source internal or external

PC Speaker Output: Yes, available on Peripheral I/O connector
LEDs: (1) System Status
Memory Bus: 8-bit data
Address Bus: 16-bit address

Power Monitoring: Dual 5% monitor – +5V and +3.3V rails
Reset hold time – 130 ms minimum, 200 ms typical
Transient voltage immunity

Manual Reset:
Available on 96-pin DIN I/O Connector
Debounced, generates minimum of 130ms reset on Low to High
Initiated by pulling Manual Reset signal line Low, then High

Memory:
DRAM EDO (soldered) memory
DRAM – EDO, 60 ns typical

Memory Options:
640 KB Main memory
EDO DRAM 60ns typical

Keyboard & Mouse:
PS/2-style or XT-style
- PS/2-style: Keyboard & optional Mouse supported
  - Keyboard provided on 96-pin Peripheral I/O connector
  - Mouse provided on 2-pin on-board header
  - 8042A compatible controller provided by PC97307
  - PS/2 serial line discipline supported
  - Open-collector bi-directional serial lines (16 mA drive)
  - 8 MHz, 12 MHz or 16 MHz serial data rates
- XT-style: Keyboard supported (there is no mouse for an XT)
  - Compatibility manufacturing option
  - Keyboard provided on 96-pin Peripheral I/O connector
  - XT compatible KBC provided by Altera CPLD

Printer/Parallel Port:
(1) Full SPP Parallel Port

Serial/RS232 Ports:
(1) or (2) 16550-compatible Serial Ports
16- or 32-byte FIFOs
Operation at all standard extended baud rates (to 115.2 Kbps), and at extended rates to 230.4 Kbps
Full EIA-RS232E and CCITT V.28 Transceivers included
- Rated to 230 Kbps
- Output swing ±9V with all Transmitter Outputs loaded with 3K ohms to Ground

Serial Two-wire RS-232:
(1) BIOS-controlled RS-232 two-wire (Rxd & Txd) Serial Port
Full EIA-RS232E and CCITT V.28 Driver & Receiver included
Output swing ±9V with all Transmitter Outputs loaded with 3K ohms to Ground

ISA Bus:
2x32 8-Bit PC® ISA bus Interface Header
Supports up to 4 external slots

SCSI Bus:
SCSI Controller, Bus Interface, and Optional Active Terminator
Optional Dallas DS21S07 Active Terminators
- Hardware enable/disable jumper option

Adaptec AIC6360 Option:
- (7) SCSI-2 devices
- SCSI BIOS included
- ASPI driver supported

System LED:
On-board system LED confirms Bios & Hardware status

Video CRT & Flat Panel: Chips and Technologies HiQ 65550 GUI Accelerator
- Complete Analog CRT Video Interface
- Complete 24-Bit Flat Panel Interface
  - provided by on-board 36-pin Header
- Compatible 8-Bit or 16-Bit Panel Interface
  - also provided on 96-Pin DIN Connector
- Monochrome (64 gray scale) or color
- Hi-Res Passive STN, Active Matrix TFT/MIM LCD, EL
- 64-bit Graphics Accelerator engine (BitBLT), H/W cursor
- VGA register set compatibility
- Supports 5V and 3.3V panels from popular manufacturers
  - such as Sharp, Optrex, Toshiba, Hitachi, Fujitsu, Samsung, NEC, Sanyo and others

2 MB Video EDO DRAM,
- 512Kx32 local bus interface
- 60 ns typical

Simultaneous CRT / Flat Panel operation supported
- using on-board 36-pin interface header for panels

Chips and Technologies drivers included

Flash Array: Soldered Flash EEPROM – 2, 4 or 8 MB

Flash Disk: Socket for user-supplied M-Systems Disk-on-Chip solid-state disk
- Support for MD2000 modules (2 to 144MB capacity)
- Coexistence support for both Flash Array and Flash Disk

Floppy Disk: Integrated Floppy Disk Controller
- (2) floppy disk drives supported
- 5.25”, 3.5” media
- 360 KB, 1.2 MB, 720 KB, 1.44 MB, 2.88 MB
- MFM (double density) or FM (single density)
- IBM MFM, ISO MFM, & Toshiba perpendicular recording formats
- 1 Mb/sec, 500 Kb/sec, 300 Kb/sec and 250 Kb/sec transfer rates
- PC8477, uDP8473, uPD765A and N82077 software compatible

Real-Time Clock, Alarm: National PC97307 – Integrated Y2K Real-Time Clock Controller
- Multi-century calendar
- On-board battery backup of RTC RAM data
- 2uA maximum draw during power-down
- Alarm & three (3) Timer Interrupts – 122 uSec to 500 mSec
- 3 bank RAM memory
  - 114 byte BIOS configuration RAM
  - 128 byte RTC configuration RAM
- Binary or BCD time formats
- 12- or 24-hour time formats
- Daylight savings time & Leap Year support

Watchdog: Dallas DS1706 Watchdog Timer/Monitor
- Software enable/disable/strobe is supported
- Minimum strobe rate while enabled – 1 strobe/second

Enable/Disable
- Defaults at power-on time to software-disabled state
- Hardware enable/disable jumper option

Connectors:

Power Connectors –
- J901: +5V supplied to Board through 96-pin DIN I/O Connector
- J003: +3.3V optionally supplied to Board through +3.3V Power Connector

J901 : Peripheral I/O Interface Connector –
- (1) 3x33 (.100 inch pitch) Right-Angle Connector
- Support top mounting (bottom by request)
- Support standard headers on request (including board stacking headers)

J902 : ISA-bus Connector –
- (1) 2x32 and pin and socket header
- stack-through and non stack-through
- board stacking is customer specified

J002 : Full Video Header –
- (1) 2x18 Header
- Support full 24-bit panels
- Support Simultaneous Video CRT and Panel Modes

J003: +3.3V Power Connector (optional)

All connectors except for the Peripheral I/O connector (J901) are optional

Peripheral I/O Signals:

Signal Pins – 96-Pin DIN Interface Connector
- Video CRT & Panel – 17
- PC Speaker – 1
- Parallel (LPT1) I/O – 17
- SCSI – 18
- Serial COM1 (RS-232E) – 8
- Serial COM2 (RS-232E) – 8
- Serial COM4 (RS-232) – 2
- Keyboard – 2
- Floppy – 15
- Reset Switch – 1
- Power & Ground

Signal Pins – Other I/O Headers
- Video Panel (Extended 36-pin Header) – 32
- Mouse Header – 2

Supply Voltage: Single supply at +5V 5%, or dual supplies at +5V 5% and +3.3V 5%

Supply Power Rating: 1W-2.5W estimated (depending upon options, excluding external peripheral requirements)

Supply Regulation: +5V and +3.3V Supplies require regulation to within 5%

Supply Rise/Fall Time: +5V Supply maximum rise time (+3V to +5V) required within 100 ms
+5V Supply maximum fall rate not to exceed 1 V/ms.

Supply Regulation: On-board regulation is provided for the on-board +3.3V supply, or optionally +3.3V supplied externally to +3.3V power connector
On-board power monitor for both 5V rail and on-board +3.3V supplies

Storage Temperature: -50C to +125C, battery excluded

Operating Temperature: Commerical 0C to +70C standard
Industrial -20C to +85C available on request
Industrial -40C to +85C available on request

Operating Software: DOS & compatible O/S

Application Software: x86 compatible

Bios Software: 128 KB or 256 KB Flash EEPROM for Bios
Bios write protection (hardware)
Chips & Technologies 65550 VGA Driver BIOS included
PC/XT compatible BIOS and Architecture

3.2 PC/II+vxe Board Block Diagram

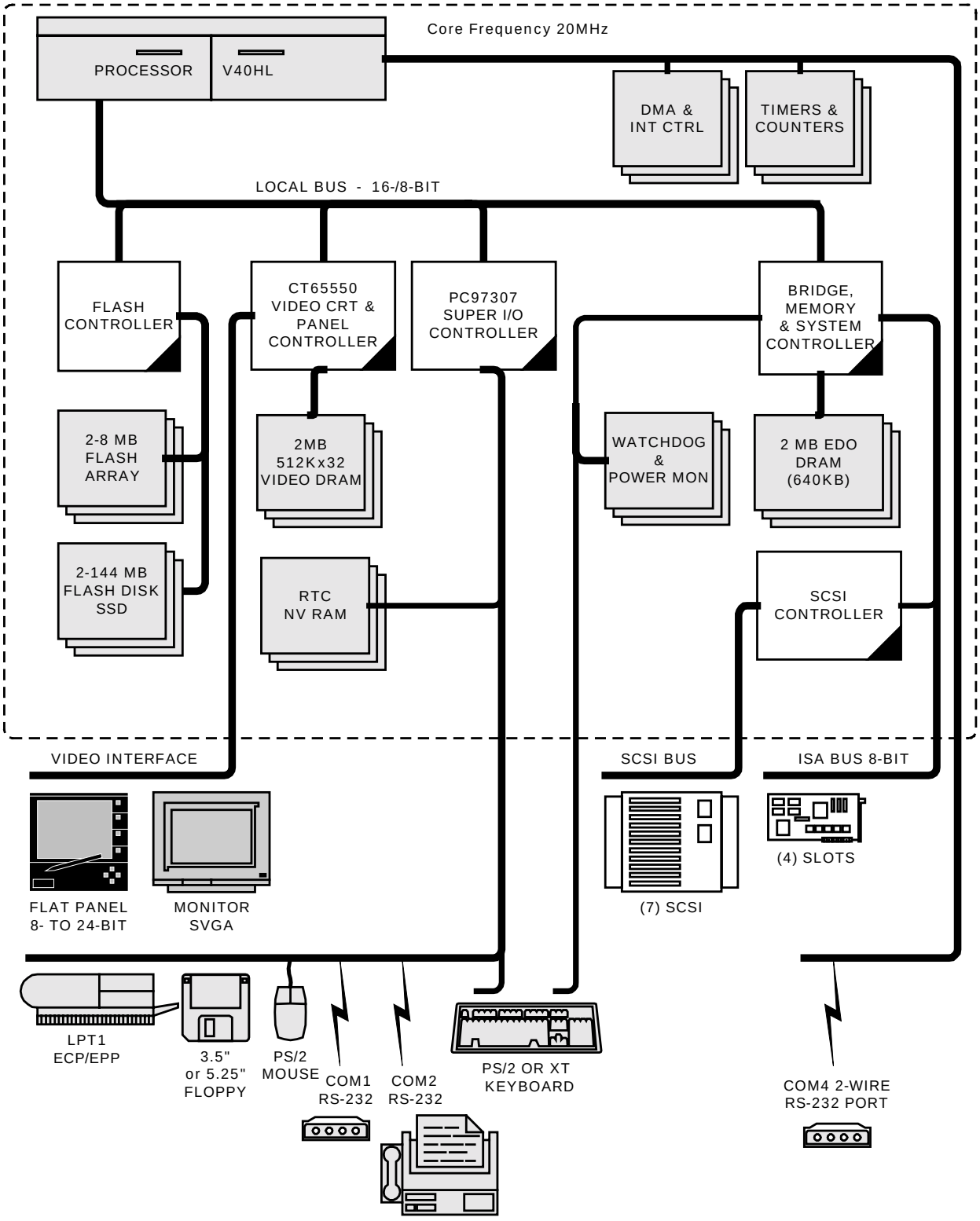


Figure 1 PC/II+vxe Block Diagram (v1.19)

4 Settings

4.1 Jumper Settings

Refer to the PC/II+vxe Component Placement diagram, section 6.2. All jumpers are on the TOP side of the board.

Table 1 Jumper Settings – Single Position Jumpers

JUMPER	SETTING	SELECTED OPTION	COMMENT
JP01	Open	Watchdog disabled	(default)
	Closed	Watchdog enabled	This option can be ordered; please refer to the Ordering Information, section 9. The watchdog controller and its internal functionality will always operate, whether or not this jumper is installed. However, the system will ONLY be forced into reset state if, at the time of a watchdog timer expiry, the watchdog is enabled by software, the timer has expired and this jumper is INSTALLED.
JP02	open	Normal operation	(default)
	closed	Reset RTC CMOS memory	Before installing this jumper (or shorting the jumper pins), VCC Power to the board should be turned off. When the jumper pins are shorted, the content of the RTC RAM Banks 0, 1 and 2 is cleared. The jumper shorts the +3V pin of the battery to Ground through a 1K resistor, and should be applied and then removed quickly before power is reapplied to the board. On reboot, default configuration parameters are restored by the BIOS. **Warning:** Use caution when handling the battery.
JP03	open	External bios	Used by Megatel manufacturing only
	closed	Normal operation	(default) Jumper must be present for normal operation.
JP04	open	Normal operation	(default)
	closed	Program bios	Used by Megatel manufacturing only

JUMPER	SETTING	SELECTED OPTION	COMMENT
JP07	open	Enable SCSI Terminator	(default) When SCSI Terminator is ordered, terminator is electrically active when shunt is NOT installed
	closed	Dsiable SCSI Terminator	When SCSI Terminator is ordered, terminator is electrically inactive when shunt is installed (Terminator enters "power-down" mode and is electrically isolated from the SCSI bus)
JP08	open	J901.C30 is Not Connected	(default) Applies when SCSI Terminator is ordered, and Option "a" specified as 2. TERMPWR is not routed to pin J901.C30; J901.C30 is unused in this case
	closed	J901.C30 is TERMPWR	Applies when SCSI Terminator is ordered, and Option "a" specified as 1. The on-board TERMPWR (termination power) line is pulled to pin J901.C30, and can be used off-board to source the SCSI bus TermPWR line.

4.2 Manufacturing Settings

Except for jumper settings, all features and options on the board are factory installed (for a complete list of manufacturing options, see section 9).

In the following tables, certain manufacturing features or options are described in more detail to assist you in selecting which setting to order. For more information, please contact your distributor or agent, or contact Megatel directly if you have specific questions or manufacturing requirements.

Table 2 Manufacturing Settings - Basic

OPTION	SETTING	SELECTED OPTION	COMMENT
Option "a"	N	SCSI Bus TermPWR Supplied by QTB	(default) JP08 is not installed and Pin J901.C30 is NOT connected to the on-board SCSI TermPWR source. Therefore the off-board SCSI bus usually sources the Scsi bus TermPWR line from some other source, eg. the transition board (QTB).
	Y	SCSI Bus TermPWR Supplied by CPU	JP08 is installed (with a shunt) and the on-board TermPWR line is connected to pin (J901.C30). This pin may therefore be used off-board to source the SCSI bus TermPWR line.
Option "b"	N	SCSI is Primary	(default) SCSI controller is primary device, I-O base is at 340h
	Y	SCSI is Secondary	SCSI controller is secondary device, I-O base is at 140h; using this option allows another SCSI controller to be used from the ISA bus which is configured as a primary controller
Option "c"	N	Watchdog H/W Disabled	(default) Watchdog is hardware disabled, board is shipped without the disable/enable jumper installed (JP01)
	Y	Watchdog H/W Enabled	Watchdog is enabled in hardware, board is shipped with the disable/enable jumper installed (JP01). In this case, the BIOS automatically disables the watchdog at boot up time, and you have the option by software of using the watchdog or not using it.

Table 3 Manufacturing Settings - Video

OPTION	SETTING	SELECTED OPTION	COMMENT
Option "h" 8-Bit Panel Type	1	J901 Panel Type is Monochrome SS 8-Bit	Monochrome SS 8-Bit Panels are supported through the 96-pin DIN Connector (J901). The 96-pin panel interface pins are mapped to the 65550 video controller pins as follows: J901.B2 (P0) is tied to 65550.P8 J901.B3 (P1) is tied to 65550.P9 J901.B4 (P2) is tied to 65550.P10 J901.A1 (P3) is tied to 65550.P11 J901.C5 (P4) is tied to 65550.P12 J901.A2 (P5) is tied to 65550.P13 J901.B6 (P6) is tied to 65550.P14 J901.C6 (P7) is tied to 65550.P15 Pins J901.A4, J901.C3, J901.C2 and J901.A5 are also used for this panel type. See notes below. 1. Pin J901.A4 (SCK) is output for all panel types from 65550.SHFCLK. 2. Pin J901.C3 is output from the 65550 pin LP/DE/BLANK# . 3. Pin J901.C2 is output from 65550 pin YD/FLM. 4. Pin J901.A5 is output from 65550 pin M/DE/BLANK#.

OPTION	SETTING	SELECTED OPTION	COMMENT
Option "h" 8-Bit Panel Type continued	2	J901 Panel Type is Color TFT 9/12-Bit	Color TFT 9 or 12-Bit Panels are supported through the 96-pin DIN Connector (J901). The 96-pin panel interface pins are mapped to the 65550 video controller pins as follows: J901.B2 (P0) is tied to 65550.P1 J901.B3 (P1) is tied to 65550.P2 J901.B4 (P2) is tied to 65550.P3 J901.A1 (P3) is tied to 65550.P4 J901.C5 (P4) is tied to 65550.P7 J901.A2 (P5) is tied to 65550.P8 J901.B6 (P6) is tied to 65550.P9 J901.C6 (P7) is tied to 65550.P10 Pins J901.A3, J901.C4, J901.A6, J901.A7, J901.A4, J901.C3, J901.C2 and J901.A5 are also used for this panel type. See notes below. 1. Pin J901.A4 (SCK) is output for all panel types from 65550.SHFCLK. 2. Pin J901.C3 (LP) is output from 65550 pin LP/DE/BLANK#; requires Manufacture Option "k" = 1 (refer to Table 2 on page 19). 3. Pin J901.C2 (FLM) is output from 65550 pin YD/FLM. 4. Pin J901.A5 (M) is output from 65550 pin M/DE/BLANK#. 5. Pin J901.A3 (P8) is output from 65550 pin P12; requires Manufacture Option "j" = 1 (refer to Table 2 on page 19). 6. Pin J901.C4 (P9) is output from 65550 pin P13. 7. Pin J901.A6 (P10) is output from 65550 pin P14. 8. Pin J901.A7 (P11) is output from 65550 pin P15.

OPTION	SETTING	SELECTED OPTION	COMMENT
Option "h" 8-Bit Panel Type continued	3	J901 Panel Type is Color STN Ext 4-Bit Packed	Pin J901.A7 (P11) is output from 65550 pin P15. Color STN Extended 4-Bit Packed panels are supported through the 96-pin DIN Connector (J901). The 96-pin panel interface pins are mapped to the 65550 video controller pins as follows: J901.B2 (P0) is tied to 65550.P0 J901.B3 (P1) is tied to 65550.P1 J901.B4 (P2) is tied to 65550.P2 J901.A1 (P3) is tied to 65550.P3 J901.C5 (P4) is tied to 65550.P4 J901.A2 (P5) is tied to 65550.P5 J901.B6 (P6) is tied to 65550.P6 J901.C6 (P7) is tied to 65550.P7 Pins J901.A4, J901.C3, J901.C2 and J901.A5 are also used for this panel type. See notes below. 1. Pin J901.A4 is output for all panel types from 65550.SHFCLK. 2. Pin J901.C3 (LP) is output from 65550 pin LP/DE/BLANK#; requires Manufacture Option "k" = 1 (refer to Table 2 on page 19). 3. Pin J901.C2 (FLM) is output from 65550 pin YD/FLM. 4. Pin J901.A5 (M) is output from 65550 pin M/DE/BLANK#.
Option "j"	1	J901.P8 is P12	J901.A3 (P8) is tied to 65550.P12. Select this option if Manufacturing Option "h" = 2
	2	J901.P8 is ENAVEE	J901.A3 (P8) is tied to 65550.ENAVEE; this signal is conditioned to be active low or active high - see option "n"
Option "k"	1	J901.M is M	J901.A5 (M) is tied to 65550.M
	2	J901.M is ENAVEE	J901.A5 (M) is tied to 65550.ENAVEE; this signal is conditioned to be active low or active high - see option "n"
Option "n"	0	ENAVEE is Active Low	The ENAVEE signal that will be output on connector pins J002.31, J901.A3 and J901.A5 will be Active Low; select this option if you will be using the compatible video interface on the 96-pin DIN connector.
	1	ENAVEE is Active High	The ENAVEE signal that will be output on connector pins J002.31, J901.A3 and J901.A5 will be Active High.

OPTION	SETTING	SELECTED OPTION	COMMENT
Option "u"	N	PS/2 Keyboard	(default) Keyboard will be PS/2 style, supported by PC97307; PS/2 mouse can also be used (if ordered)
	Y	XT Keyboard	Keyboard will be XT style, supported by Altera CPLD; no mouse is available for this XT option

5 Electrical Specifications

The PC/II+vxe board operates on a single +5V ± 5% supply, or on dual supplies of +5V ±5% and +3.3V ±5%. An onboard dual voltage monitor is used. When a single +5V supply is used, the PC/II+vxe board is shipped with either an on-board linear regulator or an on-board switching power supply to generate +3.3V.

The PC/II+vxe board is normally supplied with +5V from the 96-pin DIN connector (J901). When dual supplies option is ordered, external +3.3V is supplied to the board using the +3.3V Power Connector (J003).

5.1 Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
Power Supply	Digital	VCC	-0.3	6.0	V
Power Supply Current	(Except Peripherals Note 2)	ICC		910	mA
Ambient Temperature	**(Note 1)**	TA	-55	+125	°C
Storage Temperature	**(Note 1)**	TS	-65	+150	°C
TermPWR (SCSI) Draw	**J901.C30**	ITP		1.0	A

Warning: ***Operation at or beyond these limits may result in permanent damage to the board or to components attached to the board. Always operate the board at the Recommended Operating Conditions, see below.***

Note 1. ***Temperature is given for a board for which power is NOT applied and a Battery is NOT included onboard. If the board contains a lithium battery, then the absolute temperature board ratings must be modified to meet the more restrictive ratings for lithium batteries. Refer to manufacturer's specifications for Lithium Batteries. Never exceed the ratings of a lithium battery if a battery is present on the board.***

Note 2. ***Applies to a fully loaded board in a typical configuration, excluding additional power drawn by attached peripherals; see Table 5.3, Note 1.***

5.2 Recommended Operating Conditions

Parameter		Symbol	Min	Typical	Max	Units	*NOTES*
Power Supply	+5V Digital	VCC5	4.75	5.0	5.25	V	
	+3.3V Digital	VCC3	3.14	3.3	3.46	V	
Power Supply Rise Time	+3.0V to +5.0V	VCC5S			100	ms	
Operating Ambient Temperature	**(Note 1)**	TA	0		70	°C	(1)
Storage Ambient Temperature	**(Note 1)**	TS	-55		+125	°C	(1)
Humidity	(Untested)	HA	10		90	% RH	
PC-RSTSW# Input Level	Low Level	RSTSWL	-0.03		+0.5	V	*(2)*
PC-RSTSW# Input Level	High Level	RSTSWH	+2.8		+3.6	V	*(2)*

(1) Temperature is given for a board for which power IS applied, but a Battery is NOT included. If the board contains a lithium battery, then the absolute temperature board ratings must be modified to meet the more restrictive ratings for lithium batteries. Refer to manufacturer's specifications for Lithium Batteries. Never exceed the ratings of a lithium battery if a battery is present on the board.

(2) *Connector J901, pin A32, signal PC-**RSTSW#** (the RSTSW# input pin) drives the Dallas DS1706 Reset Switch pin. The DS1706 VCC is operated at +3.3V, and therefore **the limits specified in the above table apply to the PC/II+vxe and must NOT be exceeded**. For compatibility to other Megatel 4x4Family boards, however, and in accordance with Dallas recommendations, Megatel highly recommends that the RSTSW# line be tied to GROUND to force a reset, and otherwise be left open; in the latter case, an internal 40K resistor in the Dallas DS1706 chip pulls up the Manual Reset Switch pin to a high level during normal operation of the board.*

5.3 DC Characteristics

Over Recommended Operating Conditions

Parameter		Symbol	Min	Typical	Max	Units
Power Supply	(digital)	VCC	4.75	5.0	5.25	V
Power Supply Current		ICC		0.91		A
Power (Single Supply)	20 MHz **(Note 1,2)**	PDD5		4.1		W
Power (Dual Supplies)	+5V Rail **(Note 1)**	PDD5		3.25		W
	+3.3V Rail **(Note 1)**	PDD3		0.86		W

Note 1. ***Typical for fully loaded board, with 20 MHz processor, DRAM, 8MB Flash, Video, SCSI, IDE, Super I/O.***

Note 2. ***An on-board switching regulator supplying +3.3v to the board, regulated from the single +5V external supply.***

5.4 Voltage Monitor

An on-board micro voltage monitor is included in the PC/II+vxe board. The Dallas Semiconductor DS1706S device provides both a watchdog function and a dual-voltage monitor function. The outputs of the device are directed to the system reset bus, RST and RST#, to provide a system reset at the time of a persistent power exception. The on-board +3.3V voltage (generated locally or supplied externally to the board) is monitored at minus 5% by the primary voltage monitor, and the +5V supply is monitored by the IN input voltage sense monitor, using a precision bridge to step the +5V down to the Input Trip Point (1.25V).

Over Recommended Operating Conditions

Parameter		Symbol	Min	Typical	Max	Units
+5V Supply Voltage		VCC5	4.75	5.0	5.25	V
+3.3V Supply Voltage	External Supply	VCC3	3.15	3.3	3.45	V
IN Input Trip Point		VTP	1.20	1.25	1.30	V
VCC3 Trip Point DS1706		VCCTP	2.85	2.93	3.00	V
VCC5 Trip Point DS1706 (IN)	NOTE 1	VTP5	4.05	4.29	4.53	V
Reset Active Time		TRST	130	205	285	ms
VCC Detect to RST and RST#		TRFP	130	204	285	ms
PBRST# Stable Low to RST and RST#		TDLY			250	ms
VIN Detect to NMI#		TIPD		5	8	us

NOTES

1) The +5V supply to the board MUST be externally regulated to produce +5.0V on the board; and if +3.3V is externally supplied, the external supply must be externally regulated to produce +3.3V on the board.

6 Functional Specifications

6.1 Board Component List

The major components on the PC/II+vxe board are contained in the following table.
See Notes at the end of the table for more information.

Table 4 Board Component List

REF	QTY	DESCRIPTION [1]	PART [2]	VENDOR
BAT1	1	BATTERY – 3.0V Lithium		
CRY1	1	CRYSTAL – 14.31818 MHz		
CRY3	1	CRYSTAL – 32.768 KHz		
D004	1	LED – Isolation for SCSI Termination		
D005	1	LED – System Status Indicator		
J002	1	CONNECTOR – PANEL 24-BIT, 2X18 .100	M209981806	HARWIN
J003	1	HEADER – +3.3V Power (Optional), 1X5 .100	22-05-2051	MOLEX
J901	1	CONNECTOR – DIN R/A, 3x32 .100	86093967113 7550E1	FCI
J902	1	CONNECTOR – ISA BUS 8-BIT, 2X32 .100 Header	M20-9983206	HARWIN
JP01,JP02, JP03,JP04, JP07,JP08	6	JUMPER – 1x2 .100	M20-9990206	HARWIN
JP05	1	HEADER – MOUSE, 1X2 .100	M20-9990206	HARWIN
L006	1	INDUCTOR – for on-board 3.3V Switching Supply		
U001	1	CLOCK – Quad Programmable Clock Generator		
U002	1	MONITOR – Power Monitor & Watchdog Controller	DS1706	DALLAS
U003	1	REGULATOR – Linear Voltage Regulator	LT108x-3.3	LINEAR
U004	1	LOGIC – Gate		
U005	1	LOGIC – Bus Switch		
U006	1	PROCESSOR – x86-Compatible Cpu, 20 MHz	V40HL™	NEC
U007	1	CPLD		
U008	1	DRAM – EDO, 640 KB Memory (2MB Part), 50 ns typical	MT4LC1M16	MICRON
U009	1	LOGIC – Gate		
U011	1	FLASH ROM – ARRAY, 16Mbit (2MB) Flash	28F160	INTEL
		FLASH ROM – ARRAY, 32Mbit (4MB) Flash	28F320	INTEL
		FLASH ROM – ARRAY, 64Mbit (8MB) Flash	28F640	INTEL
U012	1	FLASH ROM – BIOS, 2Mbit (256KB) Flash	29EE020	SST
U013	1	SCSI – SCSI-2 Controller	AIC6360	ADAPTEC
U014	1	CONTROLLER – I/O, RTC, Serial x 2, Parallel, K/B & Mouse, Floppy	PC97307	NATIONAL
U015,U016	2	LINE DRIVER/RECEIVER – RS232E ESD Transceivers	ADM211E	ANALOG
U017	1	VIDEO – Video CRT/Flat Panel Controller	65550	CHIPS
U018	1	DRAM – VIDEO, EDO, 2MB Memory, 512Kx32		
U019	1	X-32 SOCKET (DIP 32-PIN) – for user-supplied Flash Disk Module		
U039	1	REGULATOR – Switching Voltage Regulator		
U040,U041	2	SCSI Active Terminators	DS21S07AE	DALLAS
U042	1	LOGIC – Inverter		
U043	1	LOGIC – Bus Switch for Video LCD/CRT		
U044	1	LOGIC – Bus Switch (2-Bit)		

NOTES

[1] For component specifications, refer to the applicable data sheets from the component respective manufacturer.

[2] All part numbers are generic, and boards may be shipped with alternatively-sourced parts which are functionally equivalent. If substitution of parts is required by Megatel, every attempt will be made to provide a functionally equivalent parts, and Megatel reserves the right to change any component on the board. Please contact your distributor or agent, or contact Megatel directly if you have specific component requirements.

6.2 Component Placement – Top Side

The following diagram shows the components on the top (component) side of the PC/II+vxe board.

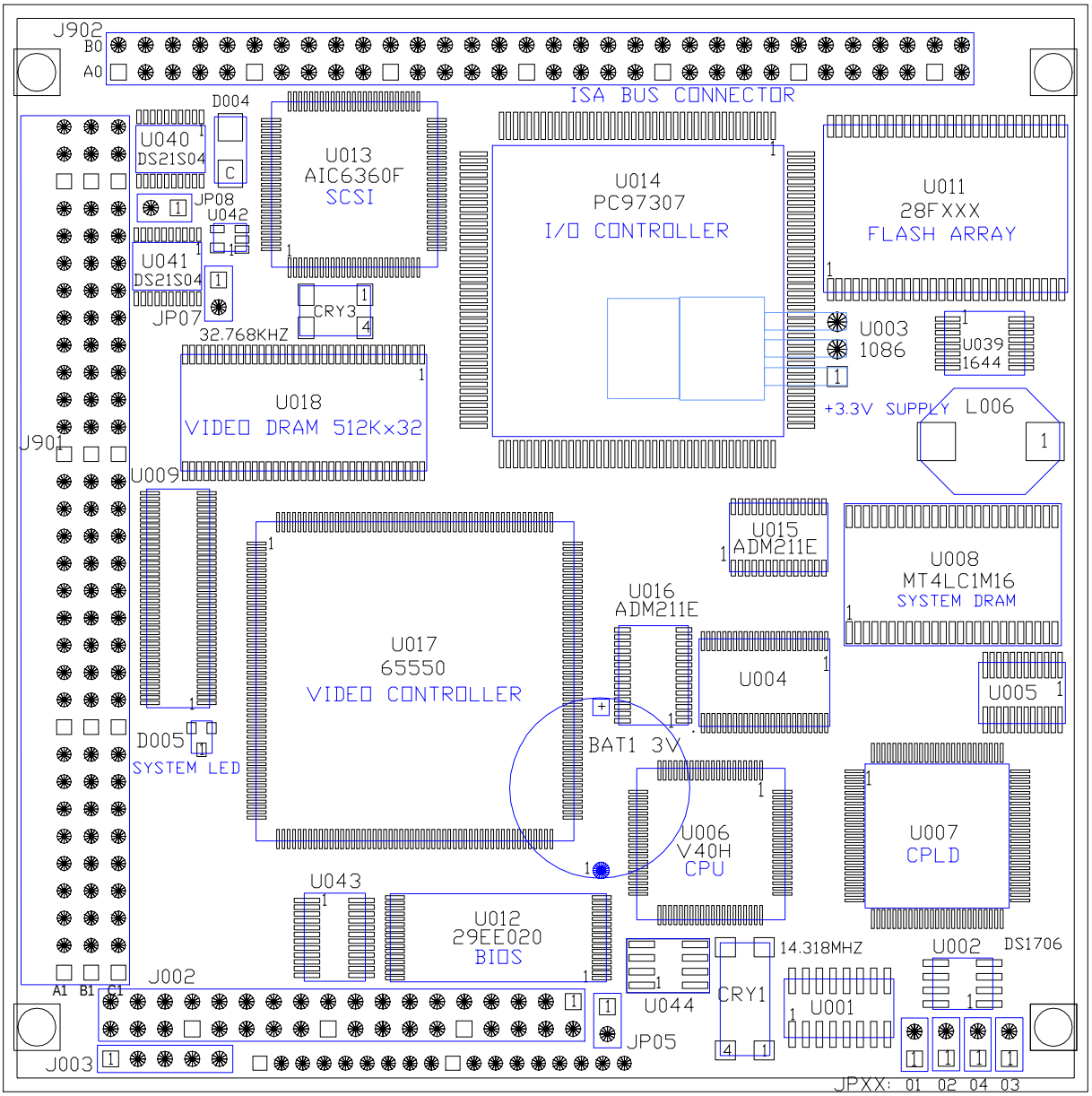


Figure 2 Component Placement – Top Side (v1.19)

6.3 Component Placement – Bottom Side

The following diagram shows the components on the bottom (solder) side of the PC/II+vxe board.

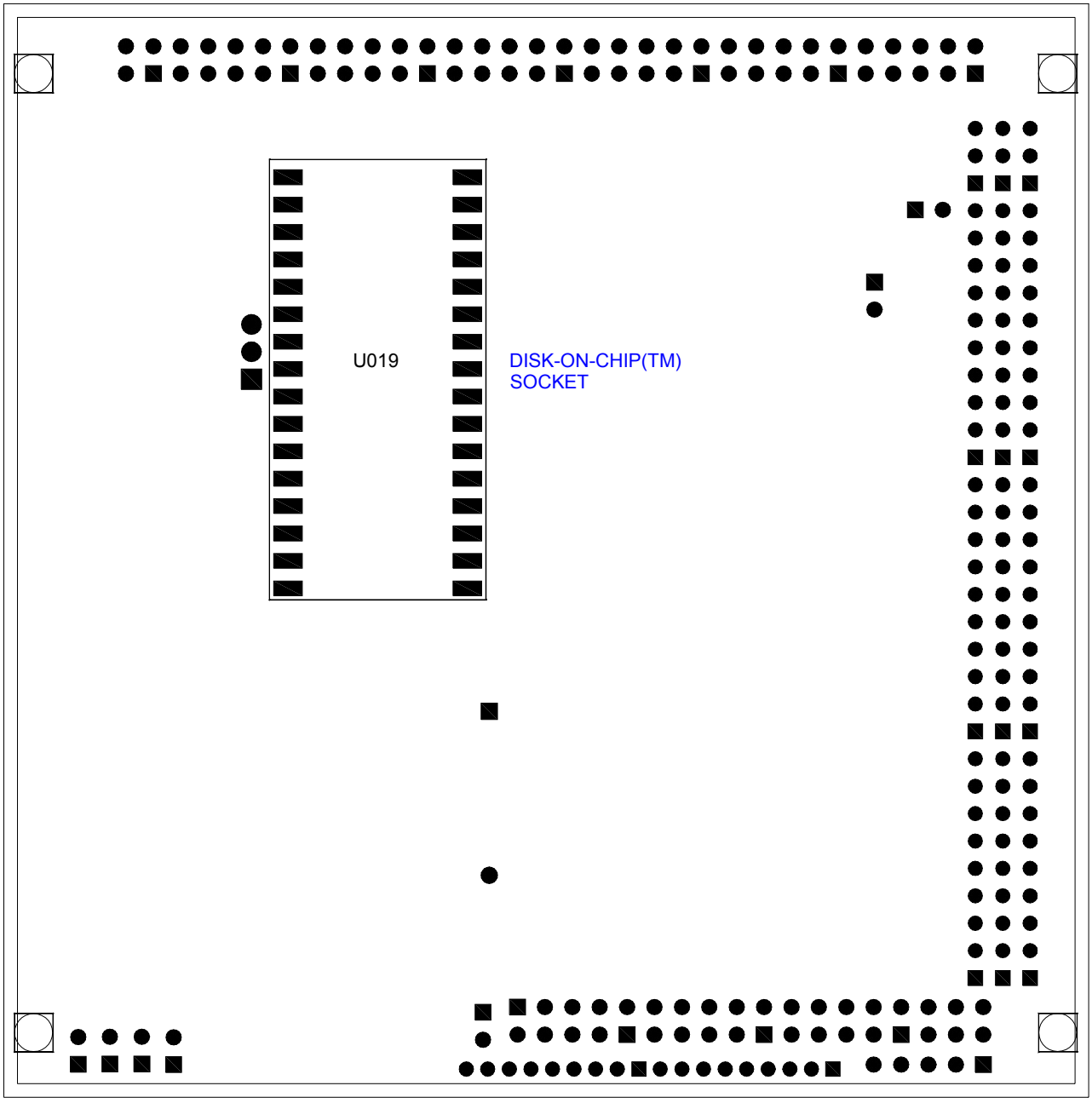


Figure 3 Component Placement – Bottom Side (v1.19)

6.4 Cpu Processor

PC/II+vxe is shipped with a x86-compatible high-performance low-power processor.

NEC V40HL™ uPD70208H 20-MHz Processor
When ordered, this processor delivers performance using a program and power efficient architecture. It provides a powerful set of features, a very complete instruction set, multiple processor emulation modes, and a set of integrated peripheral I/O and architectural units on-chip. The functional units include the following:

A. Three (3) timer channels each with a 16-bit counter, and each can be programmed in one of six (6) modes.

B. Up to 4 bus masters including an external Bus Master.

C. Wait state control for low-speed memory and I/O, automatically inserted depending upon the programmed choices made at startup. Five (5) wait state memory regions and three (3) wait state I/O regions can be specified. Automatic setting of 0 to 3 wait states can also be programmed for DMA cycles, external I/O cycles, CPU memory and Refresh cycles.

D. Up to 8 prioritized maskable interrupt request signals (7 of them external). The controller supports rotating priorities, and supports both edge-triggered and level-triggered interrupts (note that the internal timer/counter interrupt is always edge-triggered).

E. Four (4) DMA channels, supporting 20-bit addressing (1MB) and containing 16-bit transfer counters. DMA requests are maskable, operate in a variety of programmable modes, can use auto increment/decrement of the address, and provide standard TC# and END# functions.

F. Serial 2-Wire UART that is interfaced to RS-232 a driver/receiver pair. Its receive and transmit data lines are pulled to the 96-pin DIN connector (J901). The system BIOS provides support for initializing, controlling and performing I/O to this port (known as COM4 2-wire port). The Serial I/O hardware contains an on-chip dedicated baud rate generator, and provides serialization and de-serialization using standard communication parameters (data length, stop length, parity). It also supports break generation and detection, full receiver error detection and identification, and maskable interrupts.

For the V40H Cpu, refer to the NEC V40HL™ datasheet and user's manuals for more information; references to these documents can be found in the Datasheets section on page 11.

6.5 Bridge

PC/II+vxe is shipped with an on-board Bridge, Memory and System Controller provided by the CPLD (page 32).

The bridge links the local Cpu bus to the ISA bus, and is provided by the Bridge function in the CPLD. For information on the ISA bus, please see page 35.

6.6 Connectors

Connectors can be ordered by specifying one of the standard "Connector System" options (see section 9.1 for Ordering Information), or they can be custom ordered. The "Connector System" defines standard orientations which will be populated on the board for the basic connectors. Connector Options define the presence and/or detail options for each specific connector.

The following connectors are available by option:

- J901 – I/O Interface Connector – 3 x 32 (.100 inch pitch)
- J902 – ISA (8-bit) Bus Connector – 2 x 32 (.100 inch pitch)
- J002 – Panel (Full 24-bit) Connector – 2 x 18 (.100 inch pitch)
- J003 – Alternate +3.3V Power Connector – 1 X 5 (.100 inch pitch)
- JP05 – Mouse Connector – 1 x 2 (.100 inch pitch)

The "Connector System" options are:

- Option 0 – 96-pin DIN (right-angle) connector, ISA header
- Option 1 – 96-pin & ISA tall headers (for top-mounted QTB)
- Option 2 – 96-pin & ISA sockets (for bottom-mounted QTB)
- Option 3 – 96-pin DIN (right-angle) connector, no ISA connector
- Option 4 – 96-pin header, no ISA connector
- Option 5 – 96-pin stackthrough, ISA sockets, ALL on top
- Option 7 – custom connectors

In the table that follows, we specify a typical connector part number for each type of connector (header, tall header, socket, etc.). While a single source for the type of connector is given in the table, megatel may use a different part from a different supplier. If different parts are shipped by megatel, they will be compatible with the connectors given in the table that follows.

Table 5 Connector Option Part Numbers

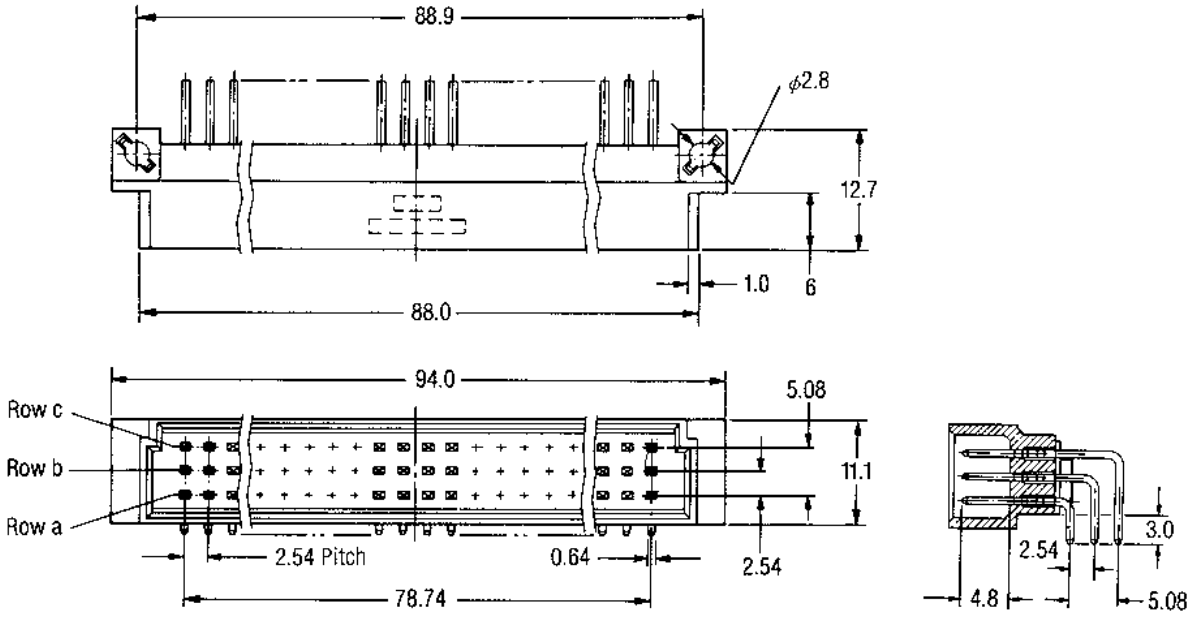
REF[1]	PINS	MOUNT	VENDOR[2]	SAMPLE PART NUMBER[2]	DESCRIPTION
J901	96	DIN R/A	FCI RN	86093967113755OE1 DIN-96CPC-SR1-TG30	3x32 .100 INCH DIN R/A MALE
		HEADER– TALL	SAMTEC	EW3209TT300	3X32 .100 INCH VERTICAL PIN
		SOCKET	SAMTEC	SLW13201TD SLW13201TS	2x32 .100 INCH VERTICAL SOCKET 1x32 .100 INCH VERTICAL SOCKET
J902	64	HEADER	HARWIN	M20-9983206	2x32 .100 INCH VERTICAL PIN
		HEADER– TALL	SAMTEC	EW3209TD300	2x32 .100 INCH VERTICAL PIN
		SOCKET	SAMTEC	SLW13201TD	2x32 .100 INCH VERTICAL SOCKET
J002	36	HEADER	HARWIN	M209981806	2x18 .100 INCH VERTICAL PIN
J003	5	HEADER	HARWIN	M20-9990506	1X5 .100 INCH HEADER
JP05	2	HEADER	HARWIN	M20-9990206	1x2 .100 INCH PIN HEADER

NOTES
[1] Nomenclature – REF is part reference number; PINS is part total pin count; MOD is connector model number, which is specified in a field of the board's part number; MOUNT is the generic location of the connector: TOP – on the top side; UP – on the top side to interconnect with a top-mounted accessory board (QTB); DOWN – on the bottom side to interconnect with a bottom-mounted accessory board (QTB).
[2] All connector part numbers are sample values; equivalent connectors may also be used.

[3] *Because a wide variety of connectors are available from a large number of sources, Megatel would be pleased to suggest mating connectors or to assist with the selection of custom connectors for your application.*

6.6.1 Eurocard DIN 41612– 0.100 Inch Centerline (Right-Angle Plug) Dimensions

The following diagram is representative of a Eurocard DIN 41612 Eurocard 3x32 pin male right-angle connector with 0.100 inch centerline pitch, as provided by AMP. AMP provide a complete line of DIN connectors that can mate to the 96-pin DIN connector used on the PC/II+vxe board. Please refer to the AMP web site, or to your AMP representative for more information.



Shown is the AMP 174111-1 3x32 0.100 inch Type C Eurocard DIN right-angle male connector. Please design to the original drawings for this connector, that are available directly from AMP and other manufacturers.

6.7 CPLD

PC/II+vxe contains an Altera CPLD that implements a Bridge (page 30) from local bus to ISA bus, a DRAM Memory Controller (page 34), and a System Controller (page 40).

The CPLD also contains the required on-board logic to allow the PC/II+vxe to function as a PC/XT architecture single-board computer.

6.8 Drivers

Refer to Flash ROM – BIOS section (page 32).

6.9 Flash ROM – BIOS

The standard ROM on the PC/II+vxe is a 2Mbit (256K Byte) flash EEPROM. A 128K Byte flash EEPROM for BIOS may also be shipped for some models.

The BIOS EEPROM contains the system BIOS and all option BIOS modules, including the SVGA BIOS, the SCSI BIOS and other bios modules required to interface to on-board peripherals. All PC/II+vxe boards are shipped with a flash BIOS.

BIOS code is mapped as follows:

1. All BIOS code is mapped into system memory address space between C0000h and FFFFFh.
2. The system BIOS code occupies the top 64 KB segment of the first 1 MB of main memory (F0000h to FFFFFh).
3. Option ROM BIOS modules are mapped into several regions located between C0000h and EFFFFh, depending upon the configuration of the PC/II+vxe board. Refer to the PC/II+vxe Memory Map table on page 51 for a complete description.

The following tables describe the drivers that are available for use with the PC/II+vxe board. Both drivers and optional ROM BIOS modules are listed. Please contact Megatel if you have specific requirements, and to receive the driver information, or visit our web site.

Table 6 VIDEO Drivers & BIOS Options

DRIVER NAME	REVISION
HiQVideo VGA BIOS	2.0.0

Table 7 FLASH Array BIOS Option

DRIVER NAME	REVISION
Datalight CardTrick (as Optional ROM)	3.01.13

6.10 Flash ROM – User

PC/II+vxe contains an optional 2MB, 4MB or 8MB of Flash Array. PC/II+vxe uses Intel® StrataFlash™ or FlashFile™ high-density symmetrically-blocked architecture flash memory. Flash Array parts are soldered on the circuit board. The flash array is supported by the Datalight Cardtrick BIOS driver (page 32).

All required programming voltages are provided on-board.

6.11 Flash Disk – M-Systems Disk-on-Chip

PC/II+vxe contains an optional 32-Pin DIP socket that can be user-populated with a M-Systems Disk-on-Chip® 2000 flash disk. The socket is bottom-mounted on the PC/II+vxe circuit board. It is the *only* part mounted on the bottom.

The Disk-on-Chip® product provides standalone or expansion Flash Disk memory in sizes ranging from 2 to 144 MB.

Both the DiskOnChip® 2000 and Flash Array can be used together on the same board.

For more detailed information on Disk-on-Chip® products, please contact M-Systems.

6.12 Floppy Disk Interface

PC/II+vxe contains an integrated Floppy Disk Drive Interface controller provided by the National PC97307, as part of the basic board. Floppy disk interface signals are pulled to J901, the Peripheral I/O Connector.

The controller supports one (1) or two (2) 3.5" or 5.25” floppy disk drives. It is compatible with standard 360 KB, 1.2 MB, 720 KB, 1.44 MB and 2.88 MB capacity disk media, and supports dual density – MFM (double density), and FM (single density).
The FDC also supports these recording formats – IBM MFM, ISO MFM, and Toshiba perpendicular recording format. The following serial transfer rates to/from the floppy device are supported – 1 Mb/sec, 500 Kb/sec, 300 Kb/sec and 250 Kb/sec.

The FDC programming interface is software compatible with these standard controllers – PC8477, uDP8473, uPD765A and N82077.

Burst and non-burst modes are supported, and a 16-byte FIFO is included.

The Floppy Disk controller uses interrupt request IRQ6, and DMA request DRQ2 (this is standard; the BIOS operates the PC97307 in legacy mode).

For more detailed information about the Floppy Disk Interface, please refer to the National PC97307 datasheet given in Reference Documents on page 11.

6.13 Interrupts

Refer to Interrupt IRQ Map on page 52 for a table of all interrupt request assignments handled by the Processor.

Refer to NMI Interrupt on page 35 for a description of the Non-Maskable interrupt.

6.14 ISA Bus

Please refer to PC® / ISA Bus Interface on page 35.

6.15 LEDs

PC/II+vxe contains a system LED that indicates (when lit) the status of the hardware. The Bios controls this LED.

6.16 Memory

The PC/II+vxe board is shipped 640 KB of Main Memory. There is a single population site on the board for a single bank of soldered-down 1Mx16 60ns (typical) EDO DRAM.

The memory controller is provided by the CPLD, and operates at zero wait-states on the 20 MHz local bus. Refer to page 32 for more information about the CPLD.

Table 8 Total System Memory – Basic Board

TOTAL	DEVICES x ORGANIZATION
640 KB	1 x 1Mx16 EDO 60ns (excess DRAM is unavailable)

NOTES
[1] Boards may be shipped with alternately-sourced parts and specifications may differ; for example, 50ns EDO parts may be shipped on some boards depending upon current availability and pricing of parts.

6.17 NMI Interrupts

The Non-maskable interrupt to the Processor is supported to report I/O Check errors that arise from the PC© Bus card slots.

The NMI is generated by the System Controller in the CPLD.

All NMI interrupts are, by default at Power Up, masked off (disabled) by the System Controller.

To enable NMI interrupts, write a value of 80h to I/O address 00A0h.
To disable NMI interrupts, write a value of 00h to I/O address 00A0h.

6.18 Parallel Port

PC/II+vxe supports a single Parallel Port controller that is integrated in the PC97307 super I/O. The parallel port is a basic feature of PC/II+vxe. It is pulled to J901, the 96-pin DIN I/O Connector.

The parallel port is managed by a 1284 controller that supports SPP mode on the parallel port interface.

LPT1 uses interrupt request IRQ7.

LPT1 is normally operated in SPP mode which does not use DMA. If LPT1 is required to operate in EPP or ECP mode, then the PC97307 PnP interface must be initialized accordingly by the user, and a DMA channel must be assigned to the Parallel Port (Logical device 4 in the PC97307) from the three available channels. In that case DRQ1 is the recommended DMA channel for this device.

For detailed specifications on the operation of the Parallel Port, please refer to the datasheet for the PC97307 given in Reference Documents on page 11.

6.19 PC® / ISA Bus Interface

The PC/II+vxe optionally supports the 8-bit ISA (PC/XT) bus. The asynchronous OSC (clock, pin B30 – refer to Table 34 Signals – J902 – ISA 8-bit Bus on page 73) signal is operated at 8.00 MHz.

An I/O read or write strobe at 3 wait states is 250 ns. Each wait state cycle (TW) is 50 ns.

A description of this bus implementation, and differences from the old PC® / XT bus, is provided in the Connectors section of this document. Please refer to section 8.2 on page 71 for the 8-bit ISA bus connector.

6.20 Real-Time Clock

The PC/II+vxe contains an optional Real-Time Clock (RTC), provided by the National PC97307 Super I/O controller. This clock is a full-function part, and is Year-2000 compliant. The RTC uses a 32.768 KHz crystal and a 3.0V Lithium battery. The battery is soldered onto the circuit board and is part of the RTC option. The Lithium battery is rated for 125 mAh (typical) in an operating range of -20C to +70C. Discharge current is 500 nA, and storage temperature is -40C to +60C.

The PC/II+vxe is factory-shipped with the Real-Time Clock set to the correct time and date for the North-American EST (Eastern Standard Time) time zone. The software for the Real-Time Clock is included in the system BIOS for boards containing the Real-Time Clock option.

The RTC is normally accessed using I/O address 0070h as an 8-bit register index, and I/O address 0071h as an 8-bit data register.

The RTC legacy interrupt request, IRQ8, is remapped by external hardware to IRQ1.

Information contained in the following sub-sections is present in summary form. For more detailed information about the Real-Time Clock, please refer to the PC97307 datasheet given in Reference Documents on page 11.

6.20.1 Features of the Real-Time Clock

- 242 Bytes battery backed up NV RAM
- Low battery current (2uA maximum power consumption during power-down)
- Century byte with Automatic Rollover & leap year provides Year 2000 compliance
- 24 or 12 Hour Format
- Programmable Alarm, Settable at Any Time hh:mm:ss, with Interrupt
- Programmable Timer, Settable to Periods Ranging from 122 uSec to 500 mSec
- Daylight Savings Time Support
- Double-buffer time registers

6.20.2 Setting Time and Date

The DOS clock is updated automatically by the Real-Time Clock upon Boot-Up. Should you change the time or date in DOS, the PC/II+vxe will conversely update the Real-Time Clock hardware time and date. The PC/II+vxe uses standard DOS instructions to change the time and date. If you are using standard DOS, and if the time and date are displayed at boot time, you may at that point change the time and date if desired. Standard DOS commands to change the TIME and DATE can also be used.

6.20.3 Using the Real-Time Clock NVRAM

The BIOS utilizes the battery backed up NVRAM to store its configuration information which it needs to access at boot time and at other times. Besides the time and data information contained in the Real-Time Clock hardware, the BIOS stores information about the Video preferences, floppy disk drive configuration, and panel information.

INDEX	BANK	# BYTES	COMMENTS
0Eh – 3Fh	All	50	
40H – 7Fh	Bank 0	64	
50h, 53h	Bank 1	128	Indirect access via 50h for address and 53h for data
TOTAL		242	

6.20.4 Real-Time Clock Interrupt 1Ah

The BIOS supports compatible real-time clock functions using software interrupt 1Ah. In addition, the PC/II+vxe BIOS supports the following functions using the software interrupt 1Ah, which provide read and write access to bank 0 and bank 1 SRAM memory in the real-time clock, and read access to the unique serial number encoded in the real-time clock chip.

1. FUNCTION 0FFh – WRITE AND READ BANK-0 SRAM

This function writes a byte to RTC SRAM Bank 0, or reads a byte from RTC SRAM Bank 0.

```
MOV    AH,0FFh
MOV    DL,<RTC bank 0 register number>
MOV    DH,<Direction>                  Bit 0 = 0 (WRITE), Bit 0 = 1 (READ)
                                       Bit 1-7 = Unused
MOV    AL,<8-Bit Value to be Written>  Used if DH.0 = 0, Unused if DH.0 = 1
INT    1Ah
-- returns here with
       /FX.CF = 1 (Error)
       /FX.CF = 0 (No Error)
              /AH = Destroyed
              /AL = value read from RTC or written to RTC>
```

2. FUNCTION 0FBh – WRITE AND READ BANK-1 EXTENDED SRAM

This function writes a byte to RTC Bank 1 Extended SRAM, or reads a byte from RTC Bank 1 Extended SRAM.

```
MOV    AH,0FBh
MOV    DL,<RTC bank 1 register number>  0 - 7Fh
MOV    DH,<Direction>                   Bit 0 = 0 (WRITE), Bit 0 = 1 (READ)
                                        Bit 1-7 = Unused
MOV    AL,<8-Bit Value to be Written>   Used if DH.0 = 0, Unused if DH.0 = 1
INT    1Ah
-- returns here with
       /FX.CF = 1 (Error)
       /FX.CF = 0 (No Error)
              /AH = Destroyed
              /AL = value read from RTC or written to RTC>
```

6.20.5 Real-Time Clock Memory Map

Table 9 Real-Time Clock Memory Map

RTC	Bank 0		Bank 1	
Offset	Description	Access	Description	Access
00	Seconds	RW	Seconds	RW
01	Seconds Alarm	RW	Seconds Alarm	RW
02	Minutes	RW	Minutes	RW
03	Minutes Alarm	RW	Minutes Alarm	RW
04	Hours	RW	Hours	RW
05	Hours Alarm	RW	Hours Alarm	RW
06	Day of the Week	RW	Day of the Week	RW
07	Day of the Month	RW	Day of the Month	RW
08	Month	RW	Month	RW
09	Year	RW	Year	RW

RTC Offset	Bank 0		Bank 1	
	Description	Access	Description	Access
0A	Register A	RW (bit 7 is read only)	Register A	RW (bit 7 is read only)
0B	Register B	RW (bit 3 is read only)	Register B	RW (bit 3 is read only)
0C	Register C	R	Register C	R
0D	Register D	R	Register D	R
0E-3F	RAM Bytes 00-3F	RW	RAM Bytes 00-3F	RW
40-47	RAM Bytes 40-47	RW	Reserved	
48	RAM Bytes 48		Century	RW
49-4F	RAM Bytes 49-4F		Reserved	
50	RAM Bytes 50		Upper RAM Address Port	RW
51-52	RAM Bytes 51-52		Reserved	
53	RAM Bytes 53		Upper RAM Data Port	RW
54-7F	RAM Bytes 54-7F		Reserved	

6.21 SCSI I/O

PC/II+vxe contains an optional SCSI controller, with on-board Dallas Active SCSI Terminators. The SCSI bus signals are pulled to J901, the 96-pin DIN I/O Connector. PC/II+vxe BIOS ships with a SCSI option BIOS module.

The SCSI interface uses interrupt request IRQ5, and DMA request DRQ0.

The Dallas DS21D07A SCSI terminators can be ordered to provide active termination of the SCSI bus on the PC/II+vxe host end of the bus. The terminators are laser-trimmed to 110 ohm at 2%, are SCSI bus hot-plug-compatible, and fully support actively negated SCSI signals. The terminators can be shunted on or off the bus electrically using a Jumper (JP07).

When the terminator is used, termination power can also be pulled to the DIN 96-pin connector from the Cpu board by inserting a shunt in Jumper JP08 (option "a" is ordered in this case) for use in sourcing TermPWR on the SCSI bus (in this case the customer uses J901.C30 to source TermPWR off-board). See page 18 for information about jumper JP08. Note that standard megatel QTB transition boards usually power the SCSI bus TermPWR line from the QTB board supply, so there is no need for the Cpu board to power the SCSI bus TermPWR line.

Adaptec AIC-6360F Controller

When ordered, the Adaptec AIC-6360 SCSI-2 controller is used as the Host device on a SCSI-2 bus at a rate up to 10 MB/sec. A 128-byte data FIFO is contained in the controller. An installable Adaptec driver (ASPI manager for DOS) is available which supports a range of devices and operating environments. For more details about the Adaptec AIC-6360 controller, refer to the Adaptec SCSI document given in Reference Documents on page 11.

6.22 Serial Ports

PC/II+vxe contains 1 or 2 optional full RS-232 ports, and an optional BIOS-accessible 2-wire RS-232 port. The serial port options include RS-232 receivers and line drivers for the respective ports which are ordered.

6.22.1 COM1 & COM2

Serial COM1 and COM2 ports are fully 16550 (with FIFOs) or 16450 (without FIFOs) compatible, and contain standard modem control and data I/O interface signals.

PC/II+vxe uses the ADM211E receiver/driver on COM1 and COM2 serial interfaces to provide RS-232 levels. The transceiver is EIA-RS232E and CCITT V.28 compliant. Input tolerance on all inputs is ±25V, and output swing on all outputs is ±9V with all transmitter outputs loaded with 3K ohms to Ground. The transceivers run at +5V and use on-chip voltage doublers and inverters. Refer to the ADM211E datasheet given in Reference Documents on page 11 for determining the power which may be drawn by attached devices.

Both ports can be operated at standard or extended baud rates of up to 230 Kbps. Each port contains both receive and transmit FIFOs which are 16-bytes or 32-bytes deep.

These two I/O ports are configured by the BIOS as COM1 and COM2.

COM1 uses interrupt request IRQ4, and is based in I/O address space at 3F8h. COM2 uses interrupt request IRQ3, and is based in I/O address space at 2F8h.

For more detailed information about serial I/O, please refer to the PC97307 datasheet given in Reference Documents on page 11.

6.22.2 COM4

A special 2-wire serial I/O port is provided by the V40 processor hardware and is supported by the PC/II+vxe BIOS. This port contains RXD and TXD (Receive Data and Transmit Data serial data signals) which are pulled out to J901, the 96-pin DIN Peripheral I/O connector.

The line driver and receiver for this port supports true RS-232 to/from CMOS voltage conversion. The driver and receiver are supported by the ADM211E shared by COM2; refer to the datasheet for this devices for more information, given in Reference Documents on page 11.

This I/O port is configured by the BIOS as COM4.

6.23 Speaker Output

Output sound waveform signals carried by the Speaker Output signal are generated by one of two sources:

1. I/O register 61h, bit 1 (Speaker Data)
2. I/O register 61h, bit 0 (Speaker Gate)

Both the Speaker Data and Speaker Gate bits must be 1, and the TCU Timer 2 must be configured to a running state to drive the speaker on. The frequency is controlled by either toggling Speaker Data on and off, or loading new counter values into TCU Timer 2.

The System Controller drives TCU TCTL2 input (which gates Timer 2), and provides a 1.19318 MHz clock input to Timer 2 (using TCLK input) by dividing a 14.31818 MHz clock by 12.

Speaker Output signal is conditioned by a driver and passed through a low pass filter, then is pulled to J901, the 96-pin DIN I/O Connector (PC-SPKROUT, pin J901.A9). It is intended to drive a piezo-electric audio transducer (a small permanent magnet speaker for example) connected between the Speaker Output signal Data pin and Ground.

6.24 Super I/O Controller

Super-I/O functionality is provided by the National PC97307 super I/O controller that is part of the basic board functionality. This controller provides 2 full 16550-style UARTs with 16-byte FIFOs (full on-board RS232 transceivers are supported), a 1284 SPP Parallel port, a PS/2-style Keyboard and PS/2 Mouse, a Real-Time clock, and a standard Floppy controller with support for two (2) 3.5” or 5.25” drives.

The functionality provided by the PC97307 Super I/O controller is described in their respective sections in this document.

6.25 System Controller

The PC/II+vxe System Controller function is implemented in the on-board Altera CPLD (page 32). This function provides an interface to the Watchdog Monitor, upper memory mapping for System BIOS, Flash Array, Flash Disk, and Video BIOS. It also provides a XT Keyboard controller and general decoding and other logic functionality, such as Speaker control and NMI control.

6.26 Timers/Counters

Three internal counters are provided by the Processor as basic features of PC/II+vxe. The timers/counters are compatible to the PC® standard 8254. The 1/2 scaled 40 MHz System Clock source (20 MHz) is used as an input to the TCU 1/4, 1/8, 1/16, or 1/32 scaler, producing 5 MHz, 2.5 MHz, 1.25 MHz or 625 KHz that can be used as the clock input for each timer/counter. An external TCLK clock source can also be made available as an option for use by any or all of the timer/counter.

Timer 0 output is tied to IRQ0 (Interrupt controller 1, level 0).
Timer 1 output is used for the two-wire serial COM4 port.
Timer 2 is used to generate signals that produce sound waveforms on the Speaker Output signal.

6.27 Video – CT 65550 Super VGA & Panel Controller

The PC/II+vxe board can be shipped with the Video option to provide the compatible video interface using the megatel 96-pin DIN connector, J901. The board can also be shipped with a new video interface connector for the 4x4Family, J002, that fully supports 8-bit through 24-bit panels. The board can also be shipped with either a 5V or a 3.3V panel interface.

The **compatible video interface** is provided on the 96-pin DIN connector, J901, and consists of either a pre-configured 8-bit, 12-bit or 16-bit panel interface, or an Analog (CRT) video interface. The panel type for this interface is ordered from the factory; refer to Order Option "h" – section 9.3.6, Option "j" – section 9.3.8, and Option "k" – section 9.3.10. The analog (CRT) interface is multiplexed on the 96-pin DIN connector (J901) with the panel signals, using the ENAVEE control signal (which is a programmable signal) to control when each is active: when ENAVEE is active, the Panel signals are presented on the connector; when ENAVEE is inactive, the Analog signals are presented on the connector.

Note that the ENAVEE signal is also made available on the 96 pin DIN connector pin A3 and A5 using options "j" and "k" respectively, and also on the LCD 24-bit panel connector, J002, pin 31. The polarity of the signal that is output to these three pins can be selected by option "n". If using the "compatible video" interface on the 96-pin DIN connector, ENAVEE should be set to active low.

The **24-bit panel interface** is provided using an on-board 2x18 .100 inch header, J002. This interface is directly interfaced to the 65550 controller, and it supports all CRT and panel types and modes supported by the C&T 65550 video controller. This interface may be used regardless of how you have specified the configuration for the "compatible video interface" (see above).

The Video Interface option includes 2MB of fast video memory EDO DRAM.

The Video panel interface can be ordered to support either 5V panels or 3.3V panels. This option affects both the 24-bit panel interface and the compatible video interface. For more information on using the 3.3V panel interface, contact Megatel Engineering.

6.27.1 Video Hardware Overview

The PC/II+vxe Video Interface uses the Chips® 65550 Video Controller and is compatible with the IBM-PS/2 Video Graphics Array (VGA) and supports the SVGA standard. The controller operates on the local bus, and supports both Analog Monitors and a wide variety of Flat Panels. It contains a powerful 64-bit Graphics Engine, Palette/DAC and Clock Synthesizer. The separate 2MB of fast EDO DRAM video memory is accessed from the controller over a direct 32-Bit bus. This video memory is used normally, to buffer all video data and is mapped by the controller into Main memory address space. It is also used for frame buffering in LCD-DD interfaces – unused video memory is automatically used for a framestore area by the controller in this case. The hardware register and gate interface is standard VGA, and the BIOS is also VGA compatible. Drivers for all common operating systems are available. Simultaneous CRT and LCD display mode is available using the on-board 36-pin LCD connector for panels and the 96-pin DIN connector for CRT.

6.27.2 Video Hardware Features

Please refer to the Chips® 65550 datasheet given in Reference Documents on page 11 for a list of features available. The 65550 supports these features (revision 1.5, December 1997):

- Highly integrated design Flat Panel and CRT GUI Accelerator & Multimedia Engine, Palette/DAC, and Clock Synthesizer
- Hardware Windows Acceleration
  - 64-bit Graphics Engine
    – System-to-Screen and Screen-to-Screen BitBLT
    – 3-Operand Raster-Ops
    – 8/16/24 Color Expansion

  - Transparent BLT
    – Optimized for Windows™ BitBLT format
- High Performance:
  - Deep write buffers
  - EDO DRAM Support
  - 40 MHz
- Display centering and stretching features for optimal fit of VGA graphics and text on 800x600 and 1024x768 panels
- Simultaneous Hardware Cursor and Pop-up Window
  - 64x64 pixels by 4 colors
  - 128x128 pixels by 2 colors
- Game Acceleration
  - Source Transparent BLT
  - Destination Transparent BLT
  - Double buffer support for YUV and 15/16bpp Overlay Engine
  - Instant Full Screen Page Flip
  - Read back of CRT Scan line counters.
- Optimized for High-Performance Flat Panel Display
  - 640x480 x 24bpp
  - 800x600 x 24bpp
  - 1024x768 x 16bpp

  CRT Support 110 MHz
- Direct interface to Color and Monochrome, Single Drive (SS), and Dual Drive (DD), STN & TFT panels
- Flexible On-chip Activity Timer facilitates ordered shut-down of the display system
- Composite NTSC / PAL Support
- Power Sequencing control outputs regulate application of Bias voltage
- Fully Compatible with IBM® VGA

6.27.3 Video Driver Features

- High Performance Accelerated drivers
- Compatible across HiQVideo family
- Auto Panning Support
- LCD/CRT/Simultaneous Mode Support
- Auto Resolution Change
- HW Stretching/Scaling
- Double Buffering
- Internationalization
- ChipsCPL (Control Panel Applet)
- Direct Draw support
- Games SDK support
- Dynamic Resolution Switching
- VGA Graphics applications in Window
- VESA DDC extensions
- VESA DPMS extensions
- Property Sheet to change Refresh/Display
- Seamless Windows Support
- Boot time resolution adjustment
- DIVE, EnDIVE
- DCAF
- DebugVGA
- Auto testing of all video modes
- ChipsVGA
- ChipsEXT

- BIOS OEM Reference Guide
- Display Driver User's Guide
- Utilities User's Guide
- Release Notes for BIOS, Drivers, and Utilities

6.27.4 Video BIOS Features

- VGA Compatible BIOS
- DDC 1, DDC 2AB
- Text and Graphics Expansion
- Auto Centering
- 44 (40) K BIOS
- CRT, LCD, Simultaneous display modes
- Auto Resolution Switch
- Multiple Refresh Rates
- NTSC/PAL support
- Extended Modes
- Extended BIOS Functions
- 1024x768 TFT, DSTN Color Panels
- Multiple Panel Support (8 panels built in)
- Get Panel Type Function
- HW Popup Interface
- Monitor Detect
- Pop Up Support
- SMI and Hot Key support
- Set Active Display Type Hook
- Save/Restore Video State Hook
- Setup Memory for Save/Restore Hook
- SMI Entry Point Hook
- Int 15 Calls after POST, Set Mode Hook

6.27.5 Video Display Enhancement Features

A variety of video enhancement features are supported, particularly for flat panels, by the Chips® 65550 Video Controller:

True-Gray

PC/II+vxe video supports TRUE-GRAY gray scale algorithm, a polynomial-based frame-rate control (FRC) and dithering algorithm to generate a maximum of 61 gray levels on monochrome panels. This algorithm extends the support of flicker-free gray scales from 16 to 61 on, for example, film-compensated monochrome STN LCDs, without the need to increase refresh rate, a conventional solution which increases power consumption, ghosting and decreases contrast.

RGB Color to Gray Scale Reduction

PC/II+vxe video supports RGB Color to Gray Scale Reduction, allowing 24-bit color pallette data to be reduced automatically to 6-bits for 64 gray scales. Reduction techniques include NTSC weighting, Equal Weighting (for blue background operating systems such as Windows), and Green Only for replicating 6-bits of green pallette data such as IBM monochrome monitors.

SmartMap

PC/II+vxe video supports SMARTMAP, an algorithm that automatically adjusts the foreground and background of adjacent gray scales to maximize contrast on flat panel displays. This algorithm is particularly useful when displaying information containing multiple colors on monochrome flat panels.

Text Enhancement

PC/II+vxe video supports Text Enhancement whereby Dim White is displayed on flat panels as Bright White to optimize contrast level.

Vertical Compensation

PC/II+vxe video supports Vertical Compensation techniques for flat panels. Unlike CRT monitors, flat panels have a fixed number of scan lines (eg. 200, 400, 480 or 768 lines). PC/II+vxe allows lower resolution software to be displayed on a higher resolution panel by use of manual or automatic Vertical Centering, Stretching, Blank Line Insertion, or Tall Font™.

Horizontal Compensation

PC/II+vxe video supports Horizontal Compensation techniques for flat panels, including Horizontal Compression, Horizontal Centering and Horizontal Doubling and text expansion.

6.27.6 Video Analog CRT Display Support

The Analog CRT interface is provided on the 96-pin DIN connector, J901, and may be used when the compatible panel interface on the 96-pin DIN connector is not being used (use of the Analog CRT video interface may occur simultaneously with a panel attached to J002, the 8/16/24-bit panel interface).

PC/II+vxe supports high resolution fixed frequency and variable frequency analog monitors in interlaced and non-interlaced modes of operation. The video controller supports up to 110 MHz, which provides SVGA resolutions up to 1280 x 1024 – 256 colors, 1024 x 768 – 256K colors or 800 x 600 – 1,677,216 colors. Please refer to the Chips® 65550 datasheet given in Reference Documents on page 11 for detailed information.

All standard VGA modes are supported on these typical CRT monitors: PS/2 fixed frequency analog CRT monitor or equivalent (31.5 / 33.5 KHz horizontal frequency specification); NEC Multi-Sync 3D or equivalent multi-frequency CRT monitor (37.5 KHz minimum horizontal frequency specification); Nanao Flexscan 9070s, Multisync 5D, or equivalent multi-frequency high-performance CRT monitor (48.5 KHz minimum horizontal frequency specification).

6.27.7 Video Flat Panel Display Support – 8/16/24-bit 2x18 Panel Connector

This section applies to panels attached to the 8/16/24-bit panel connector, J002.

The on-board Chips 65550 controller supports all flat panel display technologies, including plasma, electroluminescent (EL) and liquid crystal (LCD). LCD panel interfaces are provided for single panel, single drive (SS) and dual panel, dual drive (DD) configurations.

The controller utilizes the on-board video memory for its integrated frame buffer and 24-bit panel interface; the "C" DRAM is not used on the PC/II+vxe.

Standard and high-res passive STN and active matrix TFT/MIN LCDs are supported. Up to 16M colors on 24-bit active matrix LCDs, up to 4K colors on passive STN LCDs and up to 64 gray scales on monochrome panels are supported.

The flat panel interface can interface to a variety of panels, as illustrated in the following table; please refer to the Chips® 65550 Video Controller datasheet given in Reference Documents on page 11 for details.

Table 10 Flat Panel Interface Signal Mapping

Mass I/O Pin#	Mass I/O Pin Name	Mono SS 8-bit	Mono DD 8-bit	Mono DD 16-bit	Color TFT 9/12/ 16 bit	Color TFT 18/24 bit	Color TFT HR 18/24 bit	Color STN SS 8-bit (x4bP)	Color STN SS 16-bit (4bP)	Color STN DD 8-bit (4bP)	Color STN DD 16-bit (4bP)	Color STN DD 24-bit	65550 Pin#	65550 Pin Name
B - e6	L1-FPD0	–	UD3	UD7	B0	B0	B00	R1 - G1	R1	UR1	UR0	UR0	71	P0
B - a5	L1-FPD1	–	UD2	UD6	B1	B1	B01	B1 - R2	G1	UG1	UG0	UG0	72	P1
B - b5	L1-FPD2	–	UD1	UD5	B2	B2	B02	G2 - B2	B1	UB1	UB0	UB0	73	P2
B - c5	L1-FPD3	–	UD0	UD4	B3	B3	B03	R3 - G3	R2	UR2	UR1	LR0	74	P3
B - d5	L1-FPD4	–	LD3	UD3	B4	B4	B10	B3 - R4	G2	LR1	LR0	LG0	75	P4
B - e5	L1-FPD5	–	LD2	UD2	G0	B5	B11	G4 - B4	B2	LG1	LG0	LB0	76	P5
B - a4	L1-FPD6	–	LD1	UD1	G1	B6	B12	R5 - G5	R3	LB1	LB0	UR1	78	P6
B - b4	L1-FPD7	–	LD0	UD0	G2	B7	B13	B5 - R6	G3	LR2	LR1	UG1	79	P7
B - c4	L1-FPD8	P0	–	LD7	G3	G0	G00	SHFCLKU	B3	–	UG1	UB1	81	P8
B - d4	L1-FPD9	P1	–	LD6	G4	G1	G01	–	R4	–	UB1	LR1	82	P9
B - e4	L1-FPD10	P2	–	LD5	G5	G2	G02	–	G4	–	UR2	LG1	83	P10
B - a3	L1-FPD11	P3	–	LD4	R0	G3	G03	–	B4	–	UG2	LB1	84	P11
B - b3	L1-FPD12	P4	–	LD3	R1	G4	G10	–	R5	–	LG1	UR2	85	P12
B - c3	L1-FPD13	P5	–	LD2	R2	G5	G11	–	G5	–	LB1	UG2	86	P13
B - d3	L1-FPD14	P6	–	LD1	R3	G6	G12	–	B5	–	LR2	UB2	87	P14
B - e3	L1-FPD15	P7	–	LD0	R4	G7	G13	–	R6	–	LG2	LR2	88	P15
B - a2	L1-FPD16	–	–	–	–	R0	R00	–	–	–	–	LG2	90	P16
B - b2	L1-FPD17	–	–	–	–	R1	R01	–	–	–	–	LB2	91	P17
B - c2	L1-FPD18	–	–	–	–	R2	R02	–	–	–	–	UR3	92	P18
B - d2	L1-FPD19	–	–	–	–	R3	R03	–	–	–	–	UG3	93	P19
B - e2	L1-FPD20	–	–	–	–	R4	R10	–	–	–	–	UB3	94	P20
B - b1	L1-FPD21	–	–	–	–	R5	R11	–	–	–	–	LR3	95	P21
B - d1	L1-FPD22	–	–	–	–	R6	R12	–	–	–	–	LG3	96	P22
B - e1	L1-FPD23	–	–	–	–	R7	R13	–	–	–	–	LB3	97	P23
B - d6	L1-SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	70	SHFCLK
	Pixels/Clock	8	8	16	1	1	2	2-2/3	5-1/3	2-2/3	5-1/3	8		

NOTES
[1] The 65550 also supports panel interfaces that transfer one pixel per word, but which use both edges of SHFCLK to transfer one pixel on each edge.
[2] The higher order output lines should be used when only 9 or 12 bits are needed from the 9/12/16-bit TFT interface, or when only 18 bits are needed from the 18/24-bit TFT or TFT HR interfaces. The lower order bits should be left unconnected.
[3] The 65550 controller also supports double-clock

6.27.8 Video Mode Support – Standard VGA Modes

Which super VGA Graphics modes the Chips® 65550 can support depend upon several factors, including display memory size requirements, dot clock (display pixel rate) requirements, video DRAM memory bandwidth requirement (bytes per pixel, pixel rate and bandwidth available to the CPU). For simultaneous CRT and panel operation, compatibility between panel timing requirements and CRT requirements is also a factor. The PC/II+vxe Chips® 65550 uses a 32-bit interface to 2 MB of 50 ns (typical) EDO DRAM memory. It runs at +3.3V. The standard VGA modes supported by the PC/II+vxe are summarized in the following table.

Table 11 VGA Standard Modes Supported

Mode# (Hex)	Display Mode	Colors	Text Display	Font Size	Pixel Resolution	DotClock (MHz)	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
0, 1	Text	16	40 x 25	8x8	320x200	25.175	31.5	70
0*,1*	Text	16	40 x 25	8x14	320x350	25.175	31.5	70
0+,1+	Text	16	40 x 25	9x16	360x400	28.322	31.5	70
2,3	Text	16	80 x 25	8x8	640x200	25.175	31.5	70
2*,3*	Text	16	80 x 25	8x14	640x350	25.175	31.5	70
2+,3+	Text	16	80 x 25	9x16	720x400	28.322	31.5	70
4	Graphics	4	40 x 25	8x8	320x200	25.175	31.5	70
5	Graphics	4	40 x 25	8x8	320x200	25.175	31.5	70
6	Graphics	2	80 x 25	8x8	640x200	25.175	31.5	70
7	Text	Mono	80 x 25	9x14	720x350	25.175	31.5	70
7+	Text	Mono	80 x 25	9x16	720x400	28.322	31.5	70
D	Planar	16	40 x 25	8x8	320x200	25.175	31.5	70
D	Planar	16	80 x 25	8x8	640x200	25.175	31.5	70
F	Planar	Mono	80 x 25	8x14	640x350	25.175	31.5	70
10	Planar	16	80 x 25	8x14	640x350	25.175	31.5	70
11	Planar	2	80 x 30	8x16	640x480	25.175	31.5	60
12	Planar	16	80 x 30	8x16	640x480	25.175	31.5	60
13	Packed Pixel	256	40 x 25	8x8	320x200	25.175	31.5	70

NOTES

[1] *All of the above VGA standard modes are supported directly in the Video BIOS.*

[2] *All VGA modes using 25.175 MHz and 28.322 MHz can also be supported using 32 MHz and 36 MHz respectively.*

[3] *Extended resolution modes are not applicable to the PC/II+vxe and are not supported by the BIOS.*

6.27.9 Video Resolution, Colors, Refresh & Clocks Support – CRT, & TFT Panels

Resolution and Color Depth supported for CRT displays and/or TFT panels are contained in this section. In the following table, a representative list of the most memory bandwidth intensive resolution and color depth combinations and of the maximum screen refresh frequencies is provided. The table applies for both CRT and TFT panels, including simultaneous CRT and TFT operation. This list is not a complete list of all modes that the VGA BIOS can support. Refer to the Chips VGA BIOS documentation for more information on VGA BIOS mode support.

Table 12 Video Resolution, Colors, Refresh, & Clocks Support – CRT, & TFT Panels

Resolution and Color Depth [1]	Screen Refresh [2]	Horiz. Freq.	Dot Clock	Notes
640 x 480 x 8 bpp	85 Hz	43.3 KHz	36 MHz	
640 x 480 x 16 bpp	85 Hz	43.3 KHz	36 MHz	
640 x 480 x 24 bpp	85 Hz	43.3 KHz	36 MHz	
800 x 600 x 8 bpp	85 Hz	53.7 KHz	56.25 MHz	
800 x 600 x 16 bpp	85 Hz	53.7 KHz	56.25 MHz	
800 x 600 x 24 bpp	60 Hz	37.9 KHz	40 MHz	[3]
1024 x 768 x 8 bpp	85 Hz	68.7 KHz	94.5 MHz	
1024 x 768 x 16 bpp	56 Hz	45.2 KHz	60.7 MHz	[3]
1280 x 1024 x 8 bpp	60 Hz	64 KHz	108 MHz	

NOTES

[1] Table contents provided by the document, "Chips HiQVideo Series Mode Support", Application Note AN89, Revision 1.4, Feb 1996. Refer to the document for a list that includes all combinations supported. Except for the interlaced modes in this table, all modes apply to both CRT displays and to TFT panels, including simultaneous CRT and TFT operation.

[2] This is the maximum supported Screen Refresh frequency for the corresponding Resolution and Color Depth

[3] Mode slightly exceeds the computed bandwidth of the main display memory. However, the mode may still be supported depending on final silicon characterization and testing. Support may be possible with second-order software adjustments in the programming of the internal registers and/or somewhat reduced memory bandwidth available for CPU accesses.

6.27.10 Video Resolution, Colors, and Refresh Support – STN-DD Panels

In the following tables, a representative list of the most memory bandwidth intensive resolution and color depth combinations and of the maximum screen refresh frequencies is provided for each STN-DD panel type. Video overlay does not apply to the PC/II+vxe video interface. See notes for support of simultaneous CRT & panel operation. This list is not a complete list of all modes that the VGA BIOS can support – please refer to the Chips VGA BIOS documentation for more information on VGA BIOS mode support.

Table 13 Video Resolution, Colors & Refresh Support – STN-DD Panels

Resolution and Color Depth [1]	Screen Refresh					
	640x480 Color	640x480 Mono	800x600 Color	800x600 Mono	1024x768 Color	1024x768 Mono
640 x 480 x 8 bpp	75 Hz	75 Hz	75 Hz	75 Hz	70 Hz	70 Hz
640 x 480 x 16 bpp	85 Hz	75 Hz	75 Hz	75 Hz	70 Hz [4]	70 Hz
640 x 480 x 24 bpp	75 Hz [3]	75 Hz	75 Hz [3,4]	75 Hz [3,4]	70 Hz [5]	70 Hz [5]
800 x 600 x 8 bpp	75 Hz	75 Hz	85 Hz	75 Hz	70 Hz [3]	70 Hz
800 x 600 x 16 bpp	75 Hz	75 Hz	85 Hz [4]	75 Hz [3]	70 Hz [3,4]	70 Hz [3,4]
800 x 600 x 24 bpp	75 Hz [3]	75 Hz	85 Hz [5]	75 Hz [5]	70 Hz [3,5]	70 Hz [5]
1024 x 768 x 8 bpp	75 Hz	75 Hz	75 Hz	75 Hz	70 Hz [5]	70 Hz
1024 x 768 x 16 bpp	75 Hz	75 Hz	75 Hz [4]	75 Hz [3]	70 Hz [5]	70 Hz [5]
1280 x 1024 x 8 bpp	75 Hz	75 Hz	75 Hz	75 Hz	70 Hz [5]	70 Hz

NOTES

[1] Table contents provided by the document, "Chips HiQVideo Series Mode Support", Application Note AN89, Revision 1.4, Feb 1996. Refer to the document for a list that includes all combinations supported.

[2] This is the maximum supported Screen Refresh frequency for the corresponding Resolution and Color Depth

[3] Mode slightly exceeds the computed bandwidth of the main display memory. However, the mode may still be supported depending on final silicon characterization and testing. Support may be possible with second-order software adjustments in the programming of the internal registers and/or somewhat reduced memory bandwidth available for CPU accesses.

[4] Simultaneous CRT and panel operation is not supported. Panel-only operation can be supported (see note number 5 below).

[5] For panels, graphics raster registers and DCLK must be programmed for half the specified refresh rate, and frame acceleration must be enabled to achieve the specified panel FLM frequency. Simultaneous operation with a CRT is not supported.

[6] STN-DD panels require additional buffering compared to TFT panels and CRT displays. STN-DD panels usually are divided into upper and lower half-panels, which must be refreshed simultaneously. A “DD” buffer allows pixels to be read from display memory in a single-scan manner while refreshing the STN-DD panel in a dual-drive (“DD”) manner. In the PC/II+vxe, the DD buffer is embedded in the main display memory in an off-screen area. In this case, the DD buffer can be either full-frame or half-frame. With a half-frame DD buffer, the refresh rate of the STN-DD panel (FLM frequency) is double the refresh rate of the CRT. This doubling effect is also referred to as frame acceleration. In all of the STN-DD mode listed, frame acceleration can be used to achieve a panel refresh rate twice as high as the specified refresh rate, except in cases where frame acceleration is already assumed to be enabled.

6.28 Watchdog & Power Monitor

The PC/II+vxe contains a DS1706S Microprocessor Supervisor that provides a Watchdog timer. The Watchdog WDS# output is tied to RST# causing a minimum 200 microsecond CPU reset to occur when the watchdog timer triggers. A jumper (JP01) is included between WDS# and RST# to permanently disable the watchdog function (remove jumper to disable Watchdog, install jumper to enable watchdog function).

The Watchdog input must be driven low periodically, at a ***minimum rate of once per second***, to prevent the watchdog WDS# output from being activated. This strobe is normally driven by the PC/II+vxe board hardware, and in this mode, the watchdog does not trigger, and the Watchdog timer is in inactive mode.

To allow the Watchdog timer to trigger and cause a CPU reset, the Watchdog jumper must be inserted, the Watchdog must be activated, and the Watchdog strobe must not have been issued for a duration of 1 second.

A program-accessible interface to the Watchdog Enable/Disable control signal and the Watchdog Strobe signal are provided by the PC/II+vxe BIOS, using software interrupt 15h, functions 0FEh and 0FDh.

1. FUNCTION 0FEh – ACTIVATE AND DEACTIVATE WATCHDOG TIMER

This function activates the watchdog timer to allow software control of strobing, or deactivates the watchdog timer to disable watchdog functionality.

In ACTIVE mode the watchdog will trigger and cause a CPU reset if the watchdog jumper is inserted and a software strobe has not been issued to the watchdog in the last second using function 0FDh. Therefore, strobing at a one strobe per second rate or faster is required.

In INACTIVE mode strobing is not required and the watchdog will **not** cause a CPU reset to occur. This is the default at boot time.

```
MOV    AH,0FEh
MOV    AL,<Command>        00h = ACTIVATE watchdog
                           01h = DEACTIVATE watchdog
INT    15h
-- returns here after the specified watchdog MODE has been entered
       / ALL Registers are preserved
```

2. FUNCTION 0FDh – STROBE WATCHDOG TIMER

This function strobes the watchdog timer, causing its timer to restart. In ACTIVE mode (see function 0FEh), the watchdog must be strobed at a one strobe per second rate, and preferably at a faster rate, to prevent the watchdog timer from expiring and a CPU reset from occurring. In INACTIVE mode this function has no effect.

```
MOV    AH,0FDh
INT    15h
-- returns here after one strobe has been issued to the watchdog
       / ALL Registers are preserved
```


7 System Resource Maps

7.1 I/O Address Map

Table 14 PC/II+vxe I/O Address Map

I/O ADDRESS REGION [1]	USED BY	DESCRIPTION	USED FOR
0000-000F	CPU	DMA Controller	8237A-5
0020-0021	CPU	Interrupt Controller	8259A
0040-0043	CPU	Timer/Counter Controller	8254
0060,0064	PC97307	Keyboard & Mouse controller	8042-KBC
0061	CPLD	Speaker Control (Bits 0, 1)	SPEAKER
0070-0071	PC97307	Real-time clock	DS1287/MC146818
0080-008F	CPU	DMA page register	74LS612
00A0	CPLD	NMI Mask Register (80h=enable, 00h=disable)	NMI Mask
0102	65550	VGA global enable	BIOS
0140-015F	SCSI	SCSI controller – primary	Scsi I/O
0180-019F	CPLD	Reserved	System
0278-027A	PC97307	LPT1 (SPP mode)	Printer #1
027B-027F		Reserved	Printer #1 – EPP
02F8-02FF	PC97307	COM2-IRQ3	Serial I/O – #2
0340-035F	SCSI	SCSI controller – secondary	Scsi I/O
03B4-03B5	65550	VGA crtc index / data	VGA BIOS
03BA	65550	VGA status register / Feature Control Register	VGA BIOS
03C0-03C1	65550	VGA attrib controller index / data	VGA BIOS
03C2	65550	VGA input status register 0 / MSR	VGA BIOS
03C3	65550	VGA motherboard video system enable	VGA BIOS
03C4-03C5	65550	VGA sequence index / data	VGA BIOS
03C6-03C9	65550	VGA color palette registers	VGA BIOS
03CA	65550	VGA feature control register	VGA BIOS
03CC	65550	VGA misc output register	VGA BIOS
03CE-03CF	65550	VGA graphics controller index/data	VGA BIOS
03D0-03D1	65550	Video flat panel extension regs index/data	VGA BIOS
03D2-03D3	65550	Video multimedia extension regs index/data	VGA BIOS
03D4-03D5	65550	VGA CRTC index/data (CGA emulation)	VGA BIOS
03D6-03D7	65550	Video configuration extensions data/index	VGA BIOS
03DA	65550	VGA status register	VGA BIOS
03F0-03F7	PC97307	Primary FDC	Floppy
03F8-03FF	PC97307	COM1-IRQ4	Serial I/O – #1
0678-067D		Reserved	Printer #1 – ECP
FF00-FFDF	V40HL™	V40 Cpu - Reserved	V40
FFE0-FFFF	V40HL™	V40 Cpu - Reserved for Internal Control Registers	BNDY, WCU, REFU, BRG, Unit Allocation

NOTES
[1] Addresses are expressed in hexadecimal notation; all addresses are in the 64K physical I/O address space supported by the processor.

7.2 Memory Map

Table 15 PC/II+vxe Memory Map

MEMORY ADDRESS REGION [1]	LENGTH	DESCRIPTION
00000 – 003FF	1K	Interrupt Vector Table
00400 – 9FFFF	639K	General Use, BIOS Data, O/S, Programs
A0000 – AFFFF	64K	Video 65550 – VGA Frame Buffer
B0000 – B7FFF	32K	Video 65550 – MDA Emulation Character Buffer
B8000 – BFFFF	32K	Video 65550 – CGA Emulation Frame Buffer
C0000 – CFFFF	64K	Option BIOS Memory Address Region. This memory address region is allocated to on-board Option Video. This region is mapped to the first 64 KB page of system Flash BIOS.
D0000 – DFFFF	64K	Flash Array Memory Address Region. This memory address region is used to access any 1 of 128 – 64K user flash pages. This memory region is available for external use if the Flash Window is disabled The page numbers are assigned as follows: page 0 – 127 User flash array
E0000 – E7FFF	32K	This memory region is available for external use.
E8000 – EFFFF	32K	Flash Disk (Disk-on-Chip) Memory Address Region. This memory address region is used to access the Disk-On-Chip. Memory accesses to this region are forwarded to the on-board Disk-on-Chip. If there is no Disk-on-Chip, this memory region is available for external use.
F0000 – FFFFF	64K	BIOS ROM Memory Address Region. This memory address region is allocated to on-board BIOS Flash. This region is mapped to the fourth 64 KB page of system Flash BIOS.

NOTES
[1] *Addresses are expressed in hexadecimal notation; all addresses are in the first 1 MB of physical address space (also known as 'real memory' address region).*

7.2.1 Protection Mechanisms

The Flash Window at D0000-DFFFF, and the Disk-on-Chip Chip select are disabled by default at Power-on RESET time, and can be enabled by the BIOS.

7.3 Interrupt IRQ Map

Table 16 PC/II+vxe Interrupt Map

INTERRUPT REQUEST NUMBER [1,2,3]	SOURCE	DESCRIPTION	PC97307 LOGICAL DEVICE
IRQ0	CPU	TIMER/COUNTER-0 OUTPUT	-
IRQ1	PC97307	RTC (REMAPPED FROM IRQ8)	2
	PC97307	PS/2 KEYBOARD	0
	PC97307	PS/2 MOUSE (REMAPPED FROM IRQ12)	1
	CPLD	XT KEYBOARD	-
	CPU	COM4 (SERIAL INT OUTPUT)	-
IRQ2	-	AVAILABLE TO PC® BUS	-
	CPU	TIMER/COUNTER-1 OUTPUT	-
IRQ3	PC97307	COM2	5
IRQ4	PC97307	COM1	6
IRQ5	SCSI	SCSI CONTROLLER INTERRUPT	-
IRQ6	PC97307	FDC	3
IRQ7	PC97307	LPT1	4

NOTES
[1] Interrupt request numbers are enumerated from 0 through 7 per the conventional PC standard 8259A controller. The physical implementation of interrupt controller is internal to the CPU.
[2] The IRQ's listed in this table are assigned for use by the indicated source in default legacy mode.
[3] Interrupts are edge-triggered.

7.4 DMA Channel Map

Table 17 PC/II+vxe DMA Map

DMA REQUEST NUMBER [1]	SOURCE	DESCRIPTION
DRQ0	SCSI	SCSI I/O
DRQ1	PC97307	LPT1 [2]
	-	AVAILABLE TO PC® BUS
DRQ2	PC97307	FDC

NOTES
[1] DMA request numbers are enumerated from 0 through 3 per convention. One 4-channel DMA controller is supported by the CPU, however for the V40HL, DMA Channel 3 pin resources are shared with the V40HL SCU and therefore is unavailable for use. All DMA channels are 8-bit channels.
[2] LPT1 is normally operated in SPP mode which does not use DMA. If LPT1 is required to operate in EPP or ECP mode, then the PC97307 PnP interface must be initialized accordingly by the user, and a DMA channel must be assigned to the Parallel Port (Logical device 4 in the PC97307). In that case DRQ1 is the recommended DMA channel for this device.

8 Connector Pinouts

This section contains pinout and signal description details for each connector on the PC/II+vxe.

These connectors are described,

J901 – Peripheral I/O Connector (96-Pin Eurocard DIN)
- J901 Peripheral I/O – Power & Ground
- J901 Peripheral I/O – Serial COM1
- J901 Peripheral I/O – Serial COM2
- J901 Peripheral I/O – Serial COM4
- J901 Peripheral I/O – Floppy Disk
- J901 Peripheral I/O – Keyboard Interface
- J901 Peripheral I/O – Reset Interface
- J901 Peripheral I/O – PC Speaker Output Interface
- J901 Peripheral I/O – Parallel Port LPT1 Interface
- J901 Peripheral I/O – SCSI Bus Interface
- J901 Peripheral I/O – Video Analog (CRT–VGA) Interface
- J901 Peripheral I/O – Video Panel (8/16 Bit) Interface

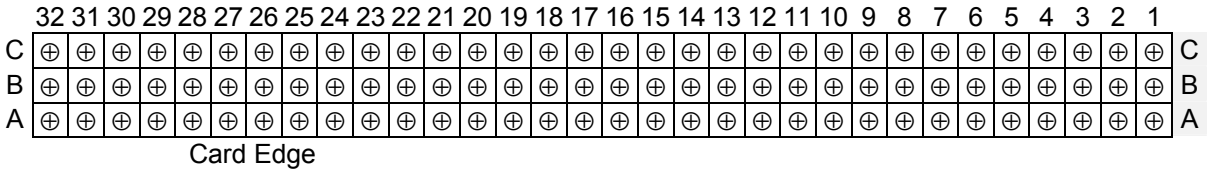
J902 – ISA Bus Connector – 8 Bit
J002 – Alternate Video 24-Bit Panel Connector – 2x18 Header
J003 – Alternate +3.3V Power Connector – 1x5 Pin Header
JP05 – Mouse Connector – 1x2 Pin Header
JP06 – Video Option Jumper Block – 2x11 2mm Pin Header

8.1 J901 – Peripheral I/O Connector (96-Pin Eurocard DIN)

This connector supplies power (+5V) to the Cpu board, and provides a peripheral interface to the following devices: Video Analog (CRT) or 8/16-bit Panel, two RS-232 Serial ports, 2-Wire RS-232 Serial Port, Parallel port, Keyboard, Floppy Disk, Printer, SCSI bus, Reset switch, and PC Speaker. Other on-board I/O is pulled to separate on-board connectors.

The Peripheral I/O connector pad area is a 3x32 .100 inch grid which can be populated with headers or connectors, one of those specified in this document or by the customer. Typically, the PC/II+vxe is shipped with the Eurocard DIN (type C) 96-pin 3-row right-angle male connector.

Figure 4 Diagram – Peripheral I/O J901 (Rows A, B, and C) – 3 X 32 .100 Eurocard DIN Connector



NOTES
[1] Top (component) view is shown. This is the view when facing a either a straight connector from the top, or a right-angle connector facing the outer side (the mating side).

Table 18 Pinout – Peripheral I/O J901 (Rows A, B, C) – 3 x 32 Eurocard DIN Connector

POS	ROW C	ROW B	ROW A
1	GND	+5V	VID-P3
2	VID-FLM V1-VSYNC	VID-P0	VID-P5
3	VID-LP V1-HSYNC	VID-P1	VID-P8
4	VID-P9 V1-G	VID-P2	VID-SCK
5	VID-P4	GND	VID-M
6	VID-P7	VID-P6	VID-P10 V1-B
7	C1-RI	C2-RI	VID-P11 V1-R
8	C1-DTR	C2-DTR	RESERVED
9	C1-CTS	C2-CTS	PC-SPKROUT
10	C1-TXD	C2-TXD	P1-SLCT
11	C1-RTS	C2-RTS	P1-PE
12	C1-RXD	C2-RXD	P1-BUSY
13	C1-DSR	C2-DSR	P1-AKN#
14	C1-DCD	C2-DCD	P1-D7
15	F1-DKCHG#	C4-RXD	P1-D6
16	F1-HDSEL#	C4-TXD	P1-D5
17	F1-RDATA#	K1-DAT	P1-D4

POS	ROW C	ROW B	ROW A
18	F1-WP#	K1-CLK	P1-D3
19	F1-TRK0#	P1-SLIN#	P1-D2
20	F1-WGATE#	P1-INIT#	P1-D1
21	F1-WDATA#	P1-ERR#	P1-D0
22	F1-STEP#	P1-AFD#	P1-STB#
23	F1-DIR#	S1-ATN#	S1-D0#
24	F1-MTR1#	S1-BSY#	S1-D1#
25	F1-DS0#	S1-AKN#	S1-D2#
26	F1-DS1#	S1-RST#	S1-D3#
27	F1-MTR0#	S1-MSG#	S1-D4#
28	F1-INDEX#	S1-SEL#	S1-D5#
29	GND	S1-C/D#	S1-D6#
30	S1_TRMPWR	S1-REQ#	S1-D7#
31	F1-DENSL0#	S1-I/O#	S1-DP#
32	GND	+5V	PC-RSTSW#

8.1.1 J901 Peripheral I/O – Power & Ground

Table 19 Signals – Peripheral I/O J901 – Power & Ground

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
+5V	B1	+5V	Power +5v
+5V	B32	+5V	Power +5v
GND	C1	Ground	Ground
GND	B5	Ground	Ground
GND	C29	Ground	Ground
GND	C32	Ground	Ground

8.1.2 J901 Peripheral I/O – Serial COM1

Table 20 Signals – Peripheral I/O J901 – Serial COM1 Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
C1-CTS	C9	Clear to Send	This active low input is the handshake signal which notifies the UART that the modem is ready to receive data.
C1-DCD	C14	Data Carrier Detect	This active low input is a handshake signal which notifies the UART that carrier signal is detected by the modem.
C1-DSR	C13	Data Set Ready	This active low input is the handshake signal which notifies the UART that the modem is ready to establish the communication link.
C1-DTR	C8	Data Terminal Ready	This active low output is the handshake output signal that signifies to modem that the UART is ready to establish data communication link.
C1-RI	C7	Ring Indicator	This active low input is the handshake signal which notifies the UART that the telephone ring signal is detected by the modem.
C1-RTS	C11	Request to Send	This Active low output is the handshake output signal that notifies the modem that the UART is ready to transmit data. The hardware reset will clear the RTS signal to inactive mode (high).
C1-RXD	C12	Receive Data	This input is the receive data serial input line, which carries RS-232 data.
C1-TXD	C10	Transmit Data	This output is the transmit data serial output line, which carries RS-232 data.

8.1.3 J901 Peripheral I/O – Serial COM2

Table 21 Signals – Peripheral I/O J901 – Serial COM2 Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
C2-CTS	B9	Clear to Send	This active low input is the handshake signal which notifies the UART that the modem is ready to receive data.
C2-DCD	B14	Data Carrier Detect	This active low input is a handshake signal which notifies the UART that carrier signal is detected by the modem.
C2-DSR	B13	Data Set Ready	This active low input is the handshake signal which notifies the UART that the modem is ready to establish the communication link.
C2-DTR	B8	Data Terminal Ready	This active low output is the handshake output signal that signifies to modem that the UART is ready to establish data communication link.
C2-RI	B7	Ring Indicator	This active low input is the handshake signal which notifies the UART that the telephone ring signal is detected by the modem.
C2-RTS	B11	Request to Send	This Active low output is the handshake output signal that notifies the modem that the UART is ready to transmit data. The hardware reset will clear the RTS signal to inactive mode (high).
C2-RXD	B12	Receive Data	This input is the receive data serial input line, which carries RS-232 data.
C2-TXD	B10	Transmit Data	This output is the transmit data serial output line, which carries RS-232 data.

8.1.4 J901 Peripheral I/O – Serial COM4

Table 22 Signals – Peripheral I/O J901 – Serial COM4 Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
C4-RXD	B15	Receive Data	This input is the receive data serial input line, which carries RS-232 data.
C4-TXD	B16	Transmit Data	This output is the transmit data serial output line, which carries RS-232 data.

8.1.5 J901 Peripheral I/O – Floppy Disk

Table 23 Signals – Peripheral I/O J901 – Floppy Disk Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
F1-DENSL0#	C31	Density Select	This signal, used with dual speed drives, when active low, reduces the spindle speed, nominally from 360rpm to 300rpm.
F1-DIR#	C23	Direction	This active low output determines the direction of the head movement (low = step-in, high = step-out). During the write or read modes, this output is high.
F1-DKCHG#	C15	Disk Change	This disk interface input indicates when the disk drive door has been opened. This active-low signal is read from bit D7 of address xx7h.
F1-DS0#	C25	Drive Select 0	Active low, output selects drive 0.
F1-DS1#	C26	Drive Select 1	Active low, output selects drive 1.
F1-HDSEL#	C16	Head Select	This active low output determines which disk drive head is active. Low = Head 0, high (open) = Head 1.
F1-INDEX#	C28	Index Status	This active low input signal senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
F1-MTR0#	C27	Motor On 0	Active-low output selects motor drive 0 (1st drive).
F1-MTR1#	C24	Motor On 1	Active-low output selects motor drive 1 (2nd drive).
F1-RDATA#	C17	Read Serial Data	This active-low, raw data read signal from the disk is connected here. Each falling edge represents a flux transition of the encoded data.
F1-STEP#	C22	Step Head	This active low output signal produces a pulse at a software-programmable rate to move the head during a seek operation.
F1-TRK0#	C19	Track 00	This active low input signal senses from the disk drive that the head is positioned over the outermost track.
F1-WDATA#	C21	Write Serial Data	This active low output is a write-precompensated serial data to be written onto the selected disk drive. Each falling edge causes a flux change on the media.
F1-WGATE#	C20	Write Gate	This active-low, high-drive output enables the write circuitry of the selected disk drive. This signal prevents glitches during power-up and power-down. This prevents writing to the disk when power is cycled.
F1-WP#	C18	Write Protected Status	This active-low input signal senses from the disk drive that a disk is write-protected. Any write command is ignored.

8.1.6 J901 Peripheral I/O – Keyboard Interface

Table 24 Signals – Peripheral I/O J901 – Keyboard Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
K1-CLK	B18	Keyboard Clock	This output is the keyboard interface clock.
K1-DAT	B17	Keyboard Data	This input is the keyboard serial data line.

8.1.7 J901 Peripheral I/O – Reset Interface

Table 25 Signals – Peripheral I/O J901 – Reset Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
PC-RSTSW#	A32	Manual Reset	Hard Reset Input, Active low. This signal drives the Manual-Reset Input. An internal 40kΩ pull-up resistor (typical) is provided on this signal line. Leave open if unused. Reset remains asserted as long as this signal is held low and for 200ms (typical; minimum 140ms) after this signal is floated. **There are two levels expected on this input line, an Active LOW level (-0.03V to +0.5V), and an Inactive HIGH level (Vcc-0.5V to Vcc+0.3V). Because of differences in CPU Supervisory chips and VCC levels, the inactive HIGH level for this line becomes dependent upon the VCC on the board and the actual Supervisory chip populated on the board.** **For compatibility with the Megatel 4x4Family, Megatel strongly recommends that this input line should be tied to GROUND to activate the RESET function, and left OPEN otherwise. Under no circumstances should this line be pulled higher than VCC+0.3V (for the PC/II+vxe, this limit is +3.6V).**

8.1.8 J901 Peripheral I/O – PC Speaker Output Interface

Table 26 Signals – Peripheral I/O J901 – PC Speaker Output Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
PC-SPKROUT	A9	Speaker Output	This signal is used to control the Speaker Output and should connect to the Speaker.

8.1.9 J901 Peripheral I/O – Parallel Port LPT1 Interface

Table 27 Signals – Peripheral I/O J901 – Parallel LPT1 Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
P1-AFD#	B22	Autofeed Output	This active low output causes the printer to automatically feed one line after each line is printed. This signal is the complement of bit 1 of the Printer Control Register.
P1-AKN#	A13	Acknowledge	This active low output from the printer indicates it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the PACK# input.
P1-BUSY	A12	Busy	This signal indicates the status of the printer. A high indicates the printer is busy and not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input.
P1-D0	A21	Port Data – Bit0	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D1	A20	Port Data – Bit1	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D2	A19	Port Data – Bit2	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D3	A18	Port Data – Bit3	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D4	A17	Port Data – Bit4	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D5	A16	Port Data – Bit5	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D6	A15	Port Data – Bit6	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D7	A14	Port Data – Bit7	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-ERR#	B21	Error	This active low signal indicates an error condition at the printer.
P1-INIT#	B20	Initiate Output	This active low signal is bit 2 of the printer control register. This is used to initiate the printer when low.
P1-PE	A11	Paper End	This signal indicates that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input.
P1-SLCT	A10	Printer Selected Status	This active high output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input.
P1-SLIN#	B19	Printer select input	This active low signal selects the printer. This is the complement of bit 3 of the Printer Control Register.

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
P1-STB#	A22	Strobe Output	This active low pulse is used to strobe the printer data into the printer. This output signal is the complement of bit 0 of the Printer Control Register.

8.1.10 J901 Peripheral I/O – SCSI Bus Interface

Table 28 Signals – Peripheral I/O J901 – SCSI Bus Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
S1-AKN#	B25	Acknowledge	A signal driven by an initiator to indicate an acknowledgment for a REQ/ACK data transfer handshake.
S1-ATN#	B23	Attention	A signal driven by an initiator to indicate the ATTENTION condition.
S1-BSY#	B24	Busy	An "OR-tied" signal that indicates that the bus is being used. It may be driven by all SCSI devices that are actually arbitrating during Arbitration, driven by the initiator, target or both during Selection & Reselection, or driven by the target during all other phases.
S1-C/D#	B29	Control/Data	A signal driven by a target that indicates whether CONTROL or DATA information is on the DATA BUS. True indicates CONTROL.
S1-D0#	A23	Data Bus Bit Signal 0	Data bit signal 0. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. S1-D1# thru S1-D8# define eight data-bit signals. Together with the S1-DP# a parity-bit signal, they form a DATA BUS. S1-D7# is the most significant bit and has the highest priority during the ARBITRATION phase. Bit number, significance, and priority decrease downward to S1-D0#.
S1-D1#	A24	Data Bus Bit Signal 1	Data bit signal 1. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-D2#	A25	Data Bus Bit Signal 2	Data bit signal 2. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-D3#	A26	Data Bus Bit Signal 3	Data bit signal 3. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-D4#	A27	Data Bus Bit Signal 4	Data bit signal 4. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-D5#	A28	Data Bus Bit Signal 5	Data bit signal 5. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-D6#	A29	Data Bus Bit Signal 6	Data bit signal 6. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
S1-D7#	A30	Data Bus Bit Signal 7	Data bit signal 7. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-DP#	A31	Data Bus Parity	Data parity bit signal. Parity is Odd. Parity is undefined during the ARBITRATION phase. See S1-D0#.
S1-I/O#	B31	Input/Output	A signal driven by a target that controls the direction of data movement on the DATA BUS with respect to an initiator. True indicates input to the initiator. This signal is also used to distinguish between SELECTION and RESELECTION phases.
S1-MSG#	B27	Message	A signal driven by a target during the MESSAGE phase.
S1-REQ#	B30	Request	A signal driven by a target to indicate a request for a REQ/ACK data transfer handshake.
S1-RST#	B26	Reset	An "OR-tied" signal that indicates the RESET condition. The RST signal may be asserted by any SCSI device at any time.
S1-SEL#	B28	Select	An "OR-tied" signal used by an initiator to select a target or by a target to reselect an initiator. NOTE: The SEL signal was not defined as "OR-tied" in SCSI-1. It has been defined as "OR-tied" in SCSI-2. This does not cause an operational problem in mixing SCSI-1 and SCSI-2 devices.
S1_TRMPWR	C30	Terminator Power	If used, connect to SCSI Bus TERMPWR line. This line is isolated from the +5V supply and decoupled on-board with a 2.2 uF Tantalum capacitor. See notes on jumper JP08 on page 18.

8.1.11 J901 Peripheral I/O – Video Analog (CRT–VGA) Interface

Table 29 Signals – Peripheral I/O J901 – Video Analog (CRT–VGA) Display Interface

PIN NAME	PIN# [1]	SIGNAL NAME	SIGNAL DESCRIPTION
V1-B	A6	CRT Blue	This Active High output signal is the BLUE CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm equivalent load on each pin (e.g. 75 ohm resistor on the board, in parallel with the 75 ohm CRT load). To enable this output signal on pin A6, install all jumper sockets into the “CRT positions” on jumper block JP06.
V1-G	C4	CRT Green	This Active High output signal is the GREEN CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm equivalent load on each pin (e.g. 75 ohm resistor on the board, in parallel with the 75 ohm CRT load). To enable this output signal on pin C4, install all jumper sockets into the “CRT positions” on jumper block JP06.
V1-HSYNC	C3	Horizontal Sync	(HSYNC or CSYNC) This Active High/Low output signal is the CRT Horizontal Sync (polarity is programmable). or the "Composite Sync" for support of various external NTSC/PAL encoder chips. To enable this output signal on pin C3, install all jumper sockets into the “CRT positions” on jumper block JP06.
V1-R	A7	CRT Red	This Active High output signal is the RED CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm equivalent load on each pin (e.g. 75 ohm resistor on the board, in parallel with the 75 ohm CRT load). To enable this output signal on pin A7, install all jumper sockets into the “CRT positions” on jumper block JP06.
V1-VSYNC	C2	Vertical Sync	(VSYNC or VISINT) This Active High/Low output signal is the CRT Vertical Sync (polarity is programmable) or "VSync Interval" for support of various external NTSC/PAL encoder chips. To enable this output signal on pin C2, install all jumper sockets into the “CRT positions” on jumper block JP06.

NOTES
[1] All pins in this table are multiplexed between CRT and Panels. For CRT operation using connector J901, ensure all of the jumper sockets are installed in the “CRT positions” in the jumper block JP06.

8.1.12 J901 Peripheral I/O – Video Panel (8/12 Bit) Interface

This section applies to the compatibility panel interface, provided on J901 (96-pin DIN connector). For a description of the full 24-bit panel interface provided on J002, please refer to section 8.3 on page 86.

To use this interface, which is compatible to that for the PC/+Vsc and compatible Cpu boards, one of the following panel type options must be ordered:

1. Monochrome SS 8-Bit Panel
2. Color TFT 9/12 Bit Panel
3. Color STN Extended 4-Bit Packed Panel

Additional custom interfaces will be announced when they become available.

Based on the ordered Panel Option, the PC/II+vxe board will be shipped with the appropriate hardware straps to support the specified panel type.

The purpose of the hardware straps is to provide the correctly mapped panel data lines on the 96-pin DIN connector. Mapping occurs from the C&T 65550 controller (used on the PC/II+vxe) to the C&T 65530 controller (used on the PC/+Vsc).

To enable panel output through J901 on the 8/12-bit interface, the ENAVEE signal must be programmed to be active.

A table for each of the optional panel types is given below. In these tables, the signal source (from the C&T 65550 controller) is given for each panel interface pin on the 96-pin DIN connector.

Table 30 Signals – Peripheral I/O J901 – Compatible Video Panel – Mono SS 8-Bit Panels

PIN NAME	PIN# [1]	SIGNAL DESCRIPTION [3]	65550 SOURCE SIGNAL [2]
VID-P0	B2	Panel Data 0. Active High. Output.	L1-FPD8
VID-P1	B3	Panel Data 1. Active High. Output.	L1-FPD9
VID-P2	B4	Panel Data 2. Active High. Output.	L1-FPD10
VID-P3	A1	Panel Data 3. Active High. Output.	L1-FPD11
VID-P4	C5	Panel Data 4. Active High. Output.	L1-FPD12
VID-P5	A2	Panel Data 5. Active High. Output.	L1-FPD13
VID-P6	B6	Panel Data 6. Active High. Output.	L1-FPD14
VID-P7	C6	Panel Data 7. Active High. Output.	L1-FPD15
VID-P8	A3		-
VID-P9 / V1-G	C4		-
VID-P10 / V1-B	A6		-
VID-P11 / V1-R	A7		-
VID-SCK	A4	Shift Clock. This signal is the pixel clock for flat panel data. Active high. Output.	L1-SHFCLK
VID-LP / V1-HSYNC	C3	Latch Pulse. Flat Panel equivalent of HSYNC. Active high. Output.	L1-LP
VID-FLM / V1-VSYNC	C2	First Line Marker. Flat Panel equivalent of VSYNC. Active high. Output.	L1-FLM
VID-M	A5	M signal. This signal is the M-signal for panel AC drive control (may also be called ACDCLK). May also be configured as BLANK# or as Display Enable (DE) for TFT Panels. Active High. Output.	L1-M

NOTES
[1] Video controller panel interface signals are multiplexed onto corresponding J901 connector output pins by jumpers in the Video Jumper block (JP06) known as CRT Mode and PANEL Mode jumpers. Only one of CRT or PANEL mode can be active across J901 at one time. Full simultaneous panel and CRT operation is supported using CRT Mode on the J901 connector, and the optional 24-bit panel connector for panels.
[2] The source signal name corresponds to the signal name assigned on the PC/II+vxe board, a description of which is provided in the 24-bit Panel Connector (2x18) Signal Table in section 8.3.
[3] The Signal Description column contains a description of the Mono SS 8-Bit panel signal attached to the corresponding 96-pin DIN connector pin.
[4] Order this Mono SS 8-Bit Panel option using code h=0; see section 9.1 on page 84.

Table 31 Signals – Peripheral I/O J901 – Compatible Video Panel – Color TFT 9/12 Bit Panels

PIN NAME	PIN# [1]	SIGNAL DESCRIPTION [2]	65550 SOURCE SIGNAL [3]
VID-P0	B2	B0. Active High. Output.	L1-FPD1 (B1)
VID-P1	B3	B1. Active High. Output.	L1-FPD2 (B2)
VID-P2	B4	B2. Active High. Output.	L1-FPD3 (B3)
VID-P3	A1	B3. Active High. Output.	L1-FPD4 (B4)
VID-P4	C5	G0. Active High. Output.	L1-FPD7 (G2)
VID-P5	A2	G1. Active High. Output.	L1-FPD8 (G3)
VID-P6	B6	G2. Active High. Output.	L1-FPD9 (G4)
VID-P7	C6	G3. Active High. Output.	L1-FPD10 (G5)
VID-P8	A3	R0. Active High. Output.	L1-FPD12 (R1)
VID-P9 / V1-G	C4	R1. Active High. Output.	L1-FPD13 (R2)
VID-P10 / V1-B	A6	R2. Active High. Output.	L1-FPD14 (R3)
VID-P11 / V1-R	A7	R3. Active High. Output.	L1-FPD15 (R4)
VID-SCK	A4	Shift Clock. This signal is the pixel clock for flat panel data. Active high. Output.	L1-SHFCLK
VID-LP / V1-HSYNC	C3	Latch Pulse. Flat Panel equivalent of HSYNC. Active high. Output.	L1-LP
VID-FLM / V1-VSYNC	C2	First Line Marker. Flat Panel equivalent of VSYNC. Active high. Output.	L1-FLM
VID-M	A5	M signal. This signal is the M-signal for panel AC drive control (may also be called ACDCLK). May also be configured as BLANK# or as Display Enable (DE) for TFT Panels. Active High. Output.	L1-M

NOTES
[1] Video controller panel interface signals are multiplexed onto corresponding J901 connector output pins by jumpers in the Video Jumper block (JP06) known as CRT Mode and PANEL Mode jumpers. Only one of CRT or PANEL mode can be active across J901 at one time. Full simultaneous panel and CRT operation is supported using CRT Mode on the J901 connector, and the optional 24-bit panel connector for panels.
[2] The Signal Description column contains a description of the Color TFT 9/12 Bit signal attached to the corresponding 96-pin DIN connector pin.
[3] The 65550 Source Signal name corresponds to the signal name assigned on the PC/II+vxe board, a description of which is provided in the 24-bit Panel Connector (2x18) Signal Table in section 8.3.
[4] Order this Color TFT 9/12 Bit Panel option using code h=1; see section 9.1 on page 84.

Table 32 Signals – Peripheral I/O J901 – Compatible Video Panel – Color STN Ext 4-Bit Pack Panels

PIN NAME	PIN# [1]	SIGNAL DESCRIPTION [3]	65550 SOURCE SIGNAL [2]
VID-P0	B2	R1 - G1. Active High. Output. In extended 4-bit pack mode, pixel values Rn-Gn-Bn are shifted into a 16-bit register every SHFCLKU period. The 8 even bits are output on P0 through P7 on the falling edge of SHFCLKU; then the 8 odd bits are output on P0 through P7 on the rising edge of SHFCLKU (the falling edge of SHFCLKL). The resulting sequence, in P0-P7 order, is R1-B1-G2-R3-B3-G4-R5-B5 G1-R2-B2-G3-R4-B4-G5-R6 For the next clock period, the next 16 bits of Rn-Gn-Bn values are shifted into the 16-bit register and output using the same packing algorithm.	L1-FPD0
VID-P1	B3	B1 - R2. Active High. Output.	L1-FPD1
VID-P2	B4	G2 - B2. Active High. Output.	L1-FPD2
VID-P3	A1	R3 - G3. Active High. Output.	L1-FPD3
VID-P4	C5	B3 - R4. Active High. Output.	L1-FPD4
VID-P5	A2	G4 - B4. Active High. Output.	L1-FPD5
VID-P6	B6	R5 - G5. Active High. Output.	L1-FPD6
VID-P7	C6	B5 - R6. Active High. Output.	L1-FPD7
VID-P8	A3		SHFCLKU
VID-P9 / V1-G	C4		-
VID-P10 / V1-B	A6		-
VID-P11 / V1-R	A7		-
VID-SCK	A4	Shift Clock. This signal is the pixel clock for flat panel data. Active high. Output.	L1-SHFCLK
VID-LP / V1-HSYNC	C3	Latch Pulse. Flat Panel equivalent of HSYNC. Active high. Output.	L1-LP
VID-FLM / V1-VSYNC	C2	First Line Marker. Flat Panel equivalent of VSYNC. Active high. Output.	L1-FLM
VID-M	A5	M signal. This signal is the M-signal for panel AC drive control (may also be called ACDCLK). May also be configured as BLANK# or as Display Enable (DE) for TFT Panels. Active High. Output.	L1-M

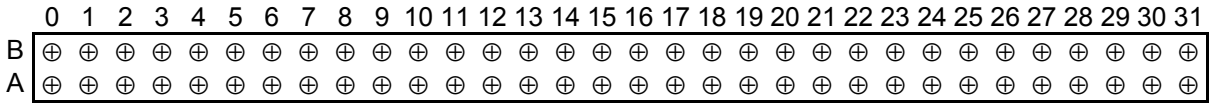
NOTES
[1] Video controller panel interface signals are multiplexed onto corresponding J901 connector output pins by jumpers in the Video Jumper block (JP06) known as CRT Mode and PANEL Mode jumpers. Only one of CRT or PANEL mode can be active across J901 at one time. Full simultaneous panel and CRT operation is supported using CRT Mode on the J901 connector, and the optional 24-bit panel connector for panels.
[2] The source signal name corresponds to the signal name assigned on the PC/II+vxe board, a description of which is provided in the 24-bit Panel Connector (2x18) Signal Table in section 8.3.
[3] The Signal Description column contains a description of the Color Extended 4-Bit Pack panel signal attached to the corresponding 96-pin DIN connector pin.
[4] Order this Color STN Ext 4-Bit Pack Panel option using code h=2; see section 9.1 on page 84.

8.2 J902 – ISA Bus Connector – 8 Bit

This section describes the 8-bit ISA Bus connector. The 64-pin (2x32) 8-bit ISA Bus connector (J902) is an option on the PC/II+vxe board.

For ISA bus signals, AC Bus termination provides termination close to the characteristic impedance of the signal line without exceeding the DC output current capabilities of the drivers. This increases data integrity and system reliability. A resistor-capacitor network of 40-60 ohms in series with 30-70 pF can be connected between each bus signal and ground. Please refer to the PC ISA Bus Specification document for additional information on the ISA bus.

Figure 5 Diagram – ISA 8-bit Bus J902 – 2 X 32 .100" Header



NOTES
[1] Top (component) view is shown.
[2] The last 31 columns (A1 through A31, and B1 through B31) of this header correspond to the PC Bus interface.
[3] Warning – the following pins used on the PC/II+vxe 8-bit ISA bus header do not correspond to those of the PC®/XT or ISA bus interface, in particular they are NOT power pins. Do NOT apply power to these pins. They are: J902.B5 (-5V) is now No Connect; J902.B7 (-12V) is now Not Connected; and J902.B9 (+12V) is now Not Connected.

Table 33 Pinout – ISA 8-bit Bus J902 (Rows A and B) – 2 X 32 .100" Header

POS [1,2]	ROW A	ROW B
0	GND	+5V
1	IOCHK#	GND
2	SD7	RESETDRV#
3	SD6	+5V
4	SD5	IRQ2
5	SD4	N/C 3
6	SD3	DRQ2
7	SD2	N/C 4
8	SD1	N/C 5
9	SD0	N/C 6
10	IORDY	GND
11	AEN	MEMW#
12	SA19	MEMR#
13	SA18	IOW#
14	SA17	IOR#
15	SA16	DACK3#
16	SA15	DRQ3
17	SA14	DACK1#
18	SA13	DRQ1
19	SA12	REFRESH#
20	SA11	BCLK
21	SA10	IRQ7
22	SA9	IRQ6
23	SA8	IRQ5
24	SA7	IRQ4
25	SA6	IRQ3
26	SA5	DACK2#
27	SA4	TC
28	SA3	BALE
29	SA2	+5V
30	SA1	OSC
31	SA0	GND

NOTES
[1] Refer to the PC®/XT or ISA Bus Specification.
[2] Pin numbering (A1-A31 and B1-B31) complies with the PC®/XT ISA 8-bit Bus Specification.
[3] Pin B5 was -5V, but has been reassigned as a No Connection.
[4] Pin B7 was -12V, but has been reassigned as a No Connection.
[5] Pin B8 was NOWS# but has been reassigned as a No Connection.
[6] Pin B9 was +12V but has been reassigned as a No Connection.

Table 34 Signals – J902 – ISA 8-bit Bus

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
ISA_+5V_1	B0	+5V	+5V
ISA_+5V_2	B3	+5V	+5V
ISA_+5V_3	B29	+5V	+5V
ISA_AEN	A11	AEN	Address Enable. Active high output. This signal is bus hold acknowledge. It is used to de-gate devices from the I/O channel to allow data transfers to take place. When asserted, I/O devices ignore the address & I/O command lines, which allows a DMA controller to proceed with a DMA transfer.
ISA_BALE	B28	BALE	Buffered Address Latch Enable. The SA address bus is valid from the falling edge of BALE to the end of the bus cycle, while the LA address bus must be latched on the falling edge of BALE.
ISA_BCLK	B20	BCLK	Bus Clock. Reference for all bus signals. This signal may vary in frequency. It can be configured in the BIOS to operate at differing frequencies, depending upon special timing requirements of attached peripherals. It is configured by default to operate at 8.00 MHz.
ISA_DACK1#	B17	DACK1#	DMA Acknowledge 1. Active Low Output. In general, this signal is raised by the DMA controller (after the DMA controller receives control of the bus from the Cpu) in response to a corresponding DMA Request signal that was asserted by a peripheral wishing to perform a DMA transfer.
ISA_DACK2#	B26	DACK2#	DMA Acknowledge 2. Active Low Output. In general, this signal is raised by the DMA controller (after the DMA controller receives control of the bus from the Cpu) in response to a corresponding DMA Request signal that was asserted by a peripheral wishing to perform a DMA transfer.
ISA_DACK3#	B15	DACK3#	DMA Acknowledge 3. Active Low Output. Tied to on-board DACK#0. In general, this signal is raised by the DMA controller (after the DMA controller receives control of the bus from the Cpu) in response to a corresponding DMA Request signal that was asserted by a peripheral wishing to perform a DMA transfer.
ISA_DRQ1	B18	DRQ1	DMA Request 1. Active high input, Asynchronous. Driven high by a peripheral to initiate DMA transfer (after the DMA controller has been appropriately programmed for a transfer), and returned to low by peripheral after DACK1# has been asserted by the DMA controller.
ISA_DRQ2	B6	DRQ2	DMA Request 2. Active high input, Asynchronous. Driven high by a peripheral to initiate DMA transfer (after the DMA controller has been appropriately programmed for a transfer), and returned to low by peripheral after DACK2# has been asserted by the DMA controller.

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
ISA_DRQ3	B16	DRQ3	DMA Request 3. Active high input, Asynchronous. Tied to on-board DRQ0. Driven high by a peripheral to initiate DMA transfer (after the DMA controller has been appropriately programmed for a transfer), and returned to low by peripheral after DACK3# has been asserted by the DMA controller.
ISA_GND1	A0	GND	Ground – 0V
ISA_GND2	B1	GND	Ground – 0V
ISA_GND3	B10	GND	Ground – 0V
ISA_GND4	B31	GND	Ground – 0V
ISA_IOCHK#	A1	IOCHK#	I/O (channel) error check condition. Active low input. When active, a non-maskable interrupt (NMI) is generated by the System Controller (CPLD) and signaled to the Cpu. I/O port 00A0h bit 7 must be set to 1 to enable NMI interrupts from the System Controller to the Cpu. IOCHK must also be enabled (port 0x61)
ISA_IOR#	B14	IOR#	I/O Read Command. Active low output. Asserted by the CPU in an I/O bus cycle, to instruct the peripheral to drive its data onto the data bus.
ISA_IORDY	A10	IORDY	I/O (channel) Ready. Active high input. When held low by a peripheral, the peripheral is preventing the bus cycle from ending. The peripheral raises this line again at the end of its bus cycle. The peripheral can therefore cause its memory or I/O cycle to be increased in length, allowing more time for it to complete the transfer. This signal should not be held low for more than 2.5 microseconds.
ISA_IOW#	B13	IOW#	I/O Write Command. Active low output. Asserted by the CPU in an I/O bus cycle, to instruct the peripheral to latch the contents of the incoming data bus.
ISA_IRQ2	B4	IRQ2	Interrupt Request Level 2. Active high input, Asynchronous. Signals an interrupt request on a low-to-high transition (if the interrupt controller level 2 has been programmed into edge-triggered mode), or when it is at a high level (if the interrupt controller level 2 has been programmed into level-triggered mode). Remains high until acknowledged (in level-triggered mode). Priorities are (highest) 0-1, 8-15, 3-7.
ISA_IRQ3	B25	IRQ3	Interrupt Request Level 3. Active high input, Asynchronous. Signals an interrupt request on a low-to-high transition (if the interrupt controller level 3 has been programmed into edge-triggered mode), or when it is at a high level (if the interrupt controller level 3 has been programmed into level-triggered mode). Remains high until acknowledged (in level-triggered mode). Priorities are (highest) 0-1, 8-15, 3-7.

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
ISA_IRQ4	B24	IRQ4	Interrupt Request Level 4. Active high input, Asynchronous. Signals an interrupt request on a low-to-high transition (if the interrupt controller level 4 has been programmed into edge-triggered mode), or when it is at a high level (if the interrupt controller level 4 has been programmed into level-triggered mode). Remains high until acknowledged (in level-triggered mode). Priorities are (highest) 0-1, 8-15, 3-7.
ISA_IRQ5	B23	IRQ5	Interrupt Request Level 5. Active high input, Asynchronous. Signals an interrupt request on a low-to-high transition (if the interrupt controller level 5 has been programmed into edge-triggered mode), or when it is at a high level (if the interrupt controller level 5 has been programmed into level-triggered mode). Remains high until acknowledged (in level-triggered mode). Priorities are (highest) 0-1, 8-15, 3-7.
ISA_IRQ6	B22	IRQ6	Interrupt Request Level 6. Active high input, Asynchronous. Signals an interrupt request on a low-to-high transition (if the interrupt controller level 6 has been programmed into edge-triggered mode), or when it is at a high level (if the interrupt controller level 6 has been programmed into level-triggered mode). Remains high until acknowledged (in level-triggered mode). Priorities are (highest) 0-1, 8-15, 3-7.
ISA_IRQ7	B21	IRQ7	Interrupt Request Level 7. Active high input, Asynchronous. Signals an interrupt request on a low-to-high transition (if the interrupt controller level 7 has been programmed into edge-triggered mode), or when it is at a high level (if the interrupt controller level 7 has been programmed into level-triggered mode). Remains high until acknowledged (in level-triggered mode). Priorities are (highest) 0-1, 8-15, 3-7.
ISA_OSC	B30	OSC	14.318 MHz, 50% duty cycle. Not synchronized to the system clock.
ISA_REFRESH#	B19	REFRESH#	Refresh. Active low input/output. Asserted by the memory refresh controller, acting as bus master, to indicate that a refresh cycle is in progress.
ISA_RESETDRV#	B2	RESETDRV#	Reset Drive. Active high output. Asserted during a system reset condition (and at power up). Synchronized to falling edge of CLK.
ISA_SA0	A31	SA0	System Address Bit 0. Bidirectional, tristate.
ISA_SA1	A30	SA1	System Address Bit 1. Bidirectional, tristate.
ISA_SA2	A29	SA2	System Address Bit 2. Bidirectional, tristate.
ISA_SA3	A28	SA3	System Address Bit 3. Bidirectional, tristate.
ISA_SA4	A27	SA4	System Address Bit 4. Bidirectional, tristate.
ISA_SA5	A26	SA5	System Address Bit 5. Bidirectional, tristate.
ISA_SA6	A25	SA6	System Address Bit 6. Bidirectional, tristate.
ISA_SA7	A24	SA7	System Address Bit 7. Bidirectional, tristate.

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
ISA_SA8	A23	SA8	System Address Bit 8. Bidirectional, tristate.
ISA_SA9	A22	SA9	System Address Bit 9. Bidirectional, tristate.
ISA_SA10	A21	SA10	System Address Bit 10. Bidirectional, tristate.
ISA_SA11	A20	SA11	System Address Bit 11. Bidirectional, tristate.
ISA_SA12	A19	SA12	System Address Bit 12. Bidirectional, tristate.
ISA_SA13	A18	SA13	System Address Bit 13. Bidirectional, tristate.
ISA_SA14	A17	SA14	System Address Bit 14. Bidirectional, tristate.
ISA_SA15	A16	SA15	System Address Bit 15. Bidirectional, tristate.
ISA_SA16	A15	SA16	System Address Bit 16. Bidirectional, tristate.
ISA_SA17	A14	SA17	System Address Bit 17. Bidirectional, tristate.
ISA_SA18	A13	SA18	System Address Bit 18. Bidirectional, tristate.
ISA_SA19	A12	SA19	System Address Bit 19. Bidirectional, tristate.
ISA_SD0	A9	SD0	System data bit 0. Active high bidirectional, tri-stated.
ISA_SD1	A8	SD1	System data bit 1. Active high bidirectional, tri-stated.
ISA_SD2	A7	SD2	System data bit 2. Active high bidirectional, tri-stated.
ISA_SD3	A6	SD3	System data bit 3. Active high bidirectional, tri-stated.
ISA_SD4	A5	SD4	System data bit 4. Active high bidirectional, tri-stated.
ISA_SD5	A4	SD5	System data bit 5. Active high bidirectional, tri-stated.
ISA_SD6	A3	SD6	System data bit 6. Active high bidirectional, tri-stated.
ISA_SD7	A2	SD7	System data bit 7. Active high bidirectional, tri-stated.
ISA_SMEMR#	B12	SMEMR#	ISA bus Memory Write Command. Active low output. Asserted if current bus cycle is an ISA memory read cycle that targets memory within the first 1MB of physical memory space. This signal is tristated when memory is addressed outside the first 1MB of physical memory space. Note – this signal is derived within the CPU from MEMR#.
ISA_SMEMW#	B11	SMEMW#	ISA bus Memory Read Command. Active low output. Asserted if current bus cycle is an ISA memory write cycle that targets memory within the first 1MB of physical memory space. This signal is tristated when memory is addressed outside the first 1MB of physical memory space. Note – this signal is derived within the CPU from MEMW#.
ISA_TC	B27	TC	Terminal Count. Active high output. The DMA controller pulses this line to indicate that the terminal count (the counter) in any DMA channel is reached, and the DMA transfer is complete.
N/C	B7		No Connection. Note – on a standard ISA bus, this pin is -12V. On the PC/II+vxe ISA bus, this is NOT a power pin.

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
N/C	B9		No Connection. Note – on a standard ISA bus, this pin is +12V. On the PC/II+vxe ISA bus, this is NOT a power pin.
N/C	B5		No Connection. Note – on a standard ISA bus, this pin is -5V. On the PC/II+vxe ISA bus, this is NOT a power pin.
N/C	B8		No Connection. Note – on a standard ISA bus, this pin is NOWS#. On the PC/II+vxe ISA bus, this is a No Connection.

NOTES
[1] *Refer to the PC®/XT ISA Bus Specification.*
[2] *Pin numbering (A1-A31 and B1-B31) complies with the PC®/XT ISA 8-bit Bus Specification.*
[3] *Pin B5 was -5V, but has been reassigned as a No Connection.*
[4] *Pin B7 was -12V, but has been reassigned as a No Connection.*
[5] *Pin B8 was NOWS# but has been reassigned as a No Connection.*
[6] *Pin B9 was +12V but has been reassigned as a No Connection.*

8.3 J002 – Alternate Video 24-Bit Panel Connector – 2x18 Header

This connector is an option for the PC/II+vxe. If used, all of the panels and modes supported by the Chips 65550 video controller can be used with this board.

Note – the compatible video interface available on J901 (the 96-pin DIN connector) supports panels and modes provided by the Chips 65530 video controller (a predecessor to the 65550). Only one panel can be attached to the PC/II+vxe regardless of which interface is used. For a description of the 8/16-bit panels supported by J901 (96-pin DIN connector), please refer to section 8.1.12 on page 65.

Table 35 Pinout – J002 – Full 24-Bit Panel Interface Header

PIN NAME [1]	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
GND	1	Ground	Ground
+5V	2	+5V	POWER +5V
L1-FPD23	3	Data Output P23	Flat panel data output P23. Active high. Output.
L1-FPD22	4	Data Output P22	Flat panel data output P22. Active high. Output.
L1-FPD21	5	Data Output P21	Flat panel data output P21. Active high. Output.
L1-FPD20	6	Data Output P20	Flat panel data output P20. Active high. Output.
L1-FPD19	7	Data Output P19	Flat panel data output P19. Active high. Output.
L1-FPD18	8	Data Output P18	Flat panel data output P18. Active high. Output.
L1-FPD17	9	Data Output P17	Flat panel data output P17. Active high. Output.
L1-FPD16	10	Data Output P16	Flat panel data output P16. Active high. Output.
L1-FPD15	11	Data Output P15	Flat panel data output P15. Active high. Output.
L1-FPD14	12	Data Output P14	Flat panel data output P14. Active high. Output.
L1-FPD13	13	Data Output P13	Flat panel data output P13. Active high. Output.
L1-FPD12	14	Data Output P12	Flat panel data output P12. Active high. Output.
L1-FPD11	15	Data Output P11	Flat panel data output P11. Active high. Output.
L1-FPD10	16	Data Output P10	Flat panel data output P10. Active high. Output.
L1-FPD9	17	Data Output P9	Flat panel data output P9. Active high. Output.
L1-FPD8	18	Data Output P8	Flat panel data output P8. Active high. Output.
L1-FPD7	19	Data Output P7	Flat panel data output P7. Active high. Output.
L1-FPD6	20	Data Output P6	Flat panel data output P6. Active high. Output.
L1-FPD5	21	Data Output P5	Flat panel data output P5. Active high. Output.
L1-FPD4	22	Data Output P4	Flat panel data output P4. Active high. Output.
L1-FPD3	23	Data Output P3	Flat panel data output P3. Active high. Output.
L1-FPD2	24	Data Output P2	Flat panel data output P2. Active high. Output.
L1-FPD1	25	Data Output P1	Flat panel data output P1. Active high. Output.
L1-FPD0	26	Data Output P0	Flat panel data output P0. Active high. Output.
L1-SHFCLK	27	Shift Clock	(SHFCLK or CL2 or SHFCLKL) This signal is the pixel clock for flat panel data. Active high. Output.
L1-LP	28	Latch Pulse	Flat Panel equivalent of HSYNC. Active high. Output.
L1-FLM	29	First Line Marker	Flat Panel equivalent of VSYNC. Active high. Output.
L1-M	30	M signal	This signal is the M-signal for panel AC drive control (may also be called ACDCLK). May also be configured as BLANK# or as Display Enable (DE) for TFT Panels. Active High. Output.
L1-ENAVEE	31	Enable VEE	(ENAVEE or ENABKL) Power sequencing controls for panel LCD bias voltage VEE, I/O. The polarity of this signal can be selected by option "n" - either active low or active high.

PIN NAME [1]	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
L1-ENAVDD	32	Enable VDD	Power sequencing controls for panel driver electronics voltage VDD. I/O.
L1-ENABKL	33	Enable Backlight	(ENBKL or A27 or GP1 or DCLK or CS) This signal is the Enable Backlight output signal. It may be configured for other functions (see Chips 65550 Datasheet – Extension Registers FR0C and FR0F and pin descriptions of MCD0-15 and A26/A27 for more information). (Chips Revision 1.5 10/14/97 65550 Subject to Change without Notice). I/O.
L1-ACTI	34	Activity Indicator	(ACTI or A26 or GP0 or DDAT or CS) This signal is the Activity Indicator output. It may be configured for other functions (see Chips 65550 Datasheet – Extension Registers FR0C and FR0F and pin descriptions of MCD0-15 and A26/A27 for more information). I/O.
GND	35	Ground	Ground
+5V	36	+5V	POWER +5V

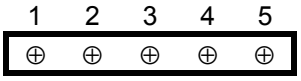
NOTES
[1] *The Pin Name is derived from the directly-attached 65550 source signal name.*

8.4 J003 – Alternate +3.3V Power Connector – 1x5 Pin Header

This connector is populated when the Dual Supplies option (Power Supply Arrangement) is ordered. All board +3.3v 5% power is supplied from an external source through this connector.

Note that when Single Supply option is ordered, J003 is not populated; instead, the board is shipped with an on-board +3.3v power supply.

Figure 6 Diagram – Alternate +3.3v Power Header J003 – 1x5 PIN .100" R/A Male Header



NOTES
[1] Top (component) view is shown.

Table 36 Pinout – Alternate +3.3v Power J003 – 1x15 PIN .100" R/A Male Header

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
+3.3V	1	+3.3V	+3.3v 5% sourced by off-board supply
GND/KEY	2	GND/KEY	Ground (or Key)
GND	3	GND	Ground
GND	4	GND	Ground
+3.3V	5	+3.3V	+3.3v 5% sourced by off-board supply

8.5 JP05 – Mouse Connector – 1x2 Pin Header

Table 37 Signals – JP05 – Mouse Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
M1-CLK	2	Mouse Clock	This output is the PS2 Mouse clock.
M1-DAT	1	Mouse Data	This input is the mouse serial data line.

9 Ordering Information

The PC/II+vxe may be ordered directly from Megatel or through one of our representatives. Inquire today! Small quantity orders (1-4) are normally available within 2 weeks. For larger orders, please allow 4 to 6 weeks for delivery.

9.1 PC/II+vxe Product Numbering

To determine the model number for a specifically configured PC/II+vxe board, use the guide below. Please contact your agent, distributor or megatel if you need assistance. There are a large number of options, and we have an easy-to-use model number calculator on our Website http://www.megatel.ca to help you.

Generic PC/II+vxe Product Number :

	Connector System	Processor	Memory		Video	Flash Array	Flash Disk-on-Chip Socket	SCSI	Real-Time Clock & Battery	Serial I/O		SCSI TermPWR Mapping	SCSI Device Assignment	Watchdog	Compatible 8/16-Bit Panel Type	8/16-bit Panel P8 Mapping	8/16-bit Panel M-Signal Mapping	ENAVEE Polarity		Keyboard Type	Mouse Header	Full 24-Bit Panel Connector	Power Supply Arrangement
PC/II+VXE/	**L**	**P**	**M**	**-**	**V**	**F**	**H**	**J**	**K**	**S**	**-**	**a**	**b**	**c**	**h**	**j**	**k**	**n**	**-**	**u**	**v**	**w**	**r**

Replace each letter following '/' by the code value given in tables below. '-'s are optional, and ‘0’s are required. Specify the full model number.

Options available (given below) are described in the following pages.

Option L – 96-pin I/O & ISA Connector System
Option P – Processor
Option M – Memory
Option V – Video
Option F – Flash Array
Option H – Flash Disk-on-Chip Socket
Option J – SCSI
Option K – Real-Time Clock & Battery
Option S – Serial
Option a – SCSI TermPWR Mapping
Option b – SCSI Device Assignment
Option c – Watchdog
Option h – Compatible 8/16-bit Panel Type
Option j – 8/16-bit Panel P8 Mapping
Option k – 8/16-bit Panel M-signal Mapping
Option n – ENAVEE Polarity
Option u – Keyboard Type
Option v – Mouse Header
Option w – Full 24-bit Panel Connector
Option r – Power Supply Arrangement

9.2 P/C/II+vxe Specific Order Example

Example :

	Connector System	Processor	Memory		Video	Flash Array	Flash Disk-on-Chip Socket	SCSI	Real-Time Clock & Battery	Serial I/O		SCSI TermPWR Mapping	SCSI Device Assignment	Watchdog	Compatible 8/16-Bit Panel Type	8/16-bit Panel P8 Mapping	8/16-bit Panel M-Signal Mapping	ENAVEE Polarity		Keyboard Type	Mouse Header	Full 24-Bit Panel Connector	Power Supply Arrangement
PC/II+VXE/	**L**	**P**	**M**	**-**	**V**	**F**	**H**	**J**	**K**	**S**	**-**	**a**	**b**	**c**	**h**	**j**	**k**	**n**	**-**	**u**	**v**	**w**	**r**
PC/II+VXE/	**0**	**1**	**1**	**-**	**1**	**3**	**1**	**1**	**1**	**3**	**-**	**0**	**0**	**2**	**1**	**0**	**0**	**1**	**-**	**1**	**0**	**1**	**1**

L=0: Connector System used is 96-pin DIN (right-angle) connector and ISA header;
P=1: NEC V40HL 20 MHz Processor;
M=1: 640 MB Soldered DRAM;
V=1: Video with 2 MB Video DRAM and 5V panel interface
F=3: 8 MB Flash Array Soldered;
H=1: Flash Disk Socket;
J=1: SCSI Bus (AIC6360) with off-board termination;
K=1: Real-Time Clock with Battery Backup installed;
S=3: 2 Serial 16550 RS-232 Channels and one 2-wire BIOS RS-232 channel;
a=0: Qtb will supply TermPWR to SCSI Bus (normal)
b=0: SCSI Configured as Primary Controller;
c=2: Watchdog Jumper & Socket Installed, h/w enabled (s/w disabled until user software enables it);
h=1: Panel Type on DIN 96-pin Connector is Color TFT 9/12-Bit;
j=0: DIN 96-pin Connector pin P8 is signal P12;
k=0: DIN 96-pin Connector pin M is signal M;
n=1: ENAVEE Polarity is Active High
u=1: Keyboard type is PS/2;
v=0: No Mouse Header;
w=1: Separate 24-Bit Panel Connector 2x18 Pin Header (J002) installed for full 24-bit panel support;
r=1: Power Supply Arrangement - Single +5v supply with linear regulator

9.3 PC/II+vxe Order Options

Options are listed in the following sub-sections, in alphabetical order of OPTION LETTER.

The following options are given below:

Option a – SCSI TermPWR Mapping
Option b – SCSI Device Assignment
Option c – Watchdog Enable
Option F – Flash Array
Option H – Flash Disk-on-Chip Socket
Option h – Compatible 8/12/16-bit Panel Type
Option J – SCSI
Option j – 8/16-bit Panel P8 Mapping
Option K – Real-Time Clock & Battery
Option k – 8/16-bit Panel M-signal Mapping
Option L – 96-pin I/O & ISA Connector System
Option M – Memory
Option n – ENAVEE Polarity
Option P – Processor
Option r – Power Supply Arrangement
Option S – Serial Channels
Option u – Keyboard Type
Option V – Video
Option v – Mouse Header (JP05)
Option w – Full 24-bit Panel Connector (J002)

9.3.1 Option a – SCSI TermPWR Mapping

0	(default) QTB SUPPLIES TERMPWR The on-board SCSI TermPWR line is NOT connected to J901.C30. This option is normal where an external transition board (QTB) supplies TermPWR to the SCSI bus. Note that in this case both the Cpu and external TermPWR supplies should be sourced by the same power supply. When this option is ordered, jumper JP08 is not installed.
1	CPU SUPPLIES TERMPWR The on-board SCSI TermPWR line is connected to J901.C30. This option is useful where an external SCSI bus has no other source for TermPWR. The SCSI TermPWR line can be sourced by the external QTB or motherboard from the Cpu board's J901.C30 pin in this case (to a maximum of 1A typical). When ordered, this option installs jumper JP08 that is populated with a shunt to allow connection of the local Cpu board TermPWR line to J901.C30 pin.

NOTES.
See Option "a" in section 4.2, page 19.
See JP09 on page 18.
See Option "J" in section 9.3.7, page 88, which explains the SCSI option.
Use 0 if no SCSI configured.

9.3.2 Option b – SCSI Device Assignment

0	SCSI is configured as Primary Controller (340), or no SCSI device selected
1	SCSI is configured as Secondary Controller (140)

NOTES.
See Option "b" in section 4.2, page 19.
See Option "J" in section 9.3.7, page 88.
Use 0 if no SCSI configured.

9.3.3 Option c – Watchdog Enabling Jumper

0	JUMPER NOT INSTALLED NO Watchdog Jumper Installed – Watchdog is Permanently Disabled
1	JUMPER INSTALLED, NO SHUNT Watchdog Jumper Installed, but Jumper Shunt is NOT installed – Watchdog is Disabled on the Shipped board (to Enable the watchdog, insert a jumper shunt on JP01 and call the Enable Watchdog BIOS function).
2	JUMPER AND SHUNT INSTALLED Watchdog Jumper Installed, and Jumper Shunt is Installed – Watchdog is ready to be used. As shipped, the BIOS will initially leave the watchdog in disabled state. To use Watchdog, call the Enable Watchdog BIOS function.

NOTES.
See Option "c" in section 4.2, page 19.
Also refer to jumper JP01 on page 17.

9.3.4 Option F – Flash Array

0	NO User Flash Array
1	2MB User Flash Array, soldered
2	4MB User Flash Array, soldered
3	8MB User Flash Array, soldered

9.3.5 Option H – Flash Disk-on-Chip Socket

0	NO Flash Disk Socket
1	Flash Disk Socket for User-supplied Disk-on-Chip module

9.3.6 Option h – Panel Type for Compatible 8/12/16-bit Interface

0	Panel Type on DIN 96-pin Connector is Monochrome SS 8-Bit
1	Panel Type on DIN 96-pin Connector is Color TFT 9/12-Bit
2	Panel Type on DIN 96-pin Connector is Color STN Ext 4-Bit Packed

NOTES.
See Option "h" in section 4.2 for a description of this option;
Also, see section 8.1.12 for a description of the connector signals for each 8/16-bit option panel.
This option does NOT affect the 24-bit panel interface connector (J002), which supports all panel types.
Use 0 if no Video configured.

9.3.7 Option J – SCSI Bus

0	NO SCSI Bus
1	SCSI Controller (Adaptec AIC-6360F SCSI-2); Termination is provided off-board
2	SCSI Controller (Adaptec AIC-6360F SCSI-2), and on-board Dallas 21S07A Active Terminators

NOTES.
SCSI bus is pulled to the Peripheral I/O connector (J901);
See section 4.2, page 19 and section 9.3.2 for selecting the SCSI device (primary or secondary);
See jumper JP08, page 18, and section 9.3.1 for selecting the Bus TermPWR Source.

9.3.8 Option j – 8/16-bit Panel P8 Mapping

0	J901.P8 is signal P12 Select this option to fully support TFT panels on the DIN 96-pin connector.
1	J901.P8 is ENAVEE

NOTES.
See Option "j" in section 4.2.
Use 0 if no Video configured.
When P8 is ENAVEE, the polarity of this signal is either active low or active high - see option "n".

9.3.9 Option K – Real-Time Clock

0	NO Real-Time Clock
1	Real-Time Clock with Battery Backup is installed

NOTES.
The Real Time Clock's RAM holds BIOS system configuration data; when not installed, the configuration data is hard-coded into the BIOS for the user. Contact Megatel Engineering for details on how to order hard-coded BIOS configuration.

9.3.10 Option k – 8/16-bit Panel M-signal Mapping

0	J901.M is M
1	J901.M is ENAVEE

NOTES.
See Option "k" in section 4.2.
Use 0 if no Video configured.
When M is ENAVEE, the polarity of this signal is either active low or active high - see option "n".

9.3.11 Option L – 96-pin I/O & ISA Connector System

0	96-pin DIN (right-angle) connector, ISA header
1	96-pin & ISA tall headers (for top-mounted QTB breakout board)
2	96-pin & ISA sockets (for bottom-mounted QTB breakout board)
3	96-pin DIN (right-angle) connector, no ISA connector
4	96-pin header, no ISA connector
5	96-pin stackthrough, ISA sockets, ALL on top
7	Custom connectors

NOTES.
J901 = 96-pin connector, J902 is 8-bit ISA connector.
Specify Custom for any other option including omitting one or more connectors.
Refer to section 6.6 on page 31 for connector descriptions.

9.3.12 Option M – Main Memory

1	DRAM 640 MB, soldered

9.3.13 Option n – ENAVEE Polarity

0	ENAVEE is Active Low
1	ENAVEE is Active High

NOTES: Affects interface connector pins J002.31, DIN96.A3(see Option "j") and DIN96.A5(see Option "k");
Select Active Low is you plan to use the compatible video interface on the 96-pin DIN connector.

9.3.14 Option P – Processor

1	NEC V40HL 20 MHz

9.3.15 Option r – Power Supply Arrangement

1	Single +5v 5% Supply; +5v supplied through J901 power pins; +3.3v generated using on-board linear regulator
2	Single +5v 5% Supply; +5v supplied through J901 power pins; +3.3v generated by on-board switching power supply
3	Dual +5v 5% and +3.3v 5% supplies; +5v supplied through J901 power pins; +3.3v supplied through J003 power pins

9.3.16 Option S – Serial Channels

0	NO Serial
1	COM1 (1) 16550 Serial Port COM1 with RS232 receivers/drivers
2	COM1, COM2 (2) 16550 Serial Ports COM1 & COM2 with RS232 receivers/drivers
3	COM1, COM2, COM4 (2) 16550 Serial Ports COM1 & COM2 with RS232 receivers/drivers; and (1) 2-Wire BIOS Serial Port COM4 with RS232 receiver/driver

9.3.17 Option u – Keyboard Type

1	Keyboard is PS/2 Style (PC/AT)
2	Keyboard is XT Style (PC/XT)

NOTES.
See Option "u", in Manufacturing Settings, page 19.
A mouse may only be ordered when a PS/2-style (PC/AT) keyboard controller is ordered.
Therefore if u = 2 (PC/XT keyboard) is selected, then you must select v = 0 (no mouse).

9.3.18 Option V – Video

0	NO Video
1	Video Option with +5V Panel/CRT Interface. Includes 2MB Video Memory; CRT and 8/16-bit panel interfaces are pulled to the Peripheral I/O Connector; 24-bit panel interfaces are pulled to a separate 24-bit panel connector.
2	Video Option with +3.3V Panel/CRT Interface. Same features as above.

9.3.19 Option v – Mouse Header (JP05)

0	NO Mouse Header
1	Mouse Header (1x2 .100 inch Header)

NOTES.
See Option "u", in Manufacturing Settings, page 19.
If v = 1 is selected, then you must select u = 1 (PS/2 style).

9.3.20 Option w – Full 24-bit Panel Connector (J002)

0	NO 24-bit Panel Connector (J002)
1	24-Bit Panel Connector 2x18 Pin Header (J002)
C	Custom 24-bit Panel Connector

NOTES.
This connector is an alternative 24-bit panel interface to the 8/16-bit panel interface provided by J901.
The interface on J901 provides a compatible option panel interface that is limited to 8-bit to 16-bit panels.
Only (1) panel may be active on a board regardless of whether either or both J901 and J002 are ordered.
CRTs are attached using J901 and multiplex with the 8/16-bit Panel interface on J901 (software selectable).

10 Service Information

If you feel your board requires service, Megatel Service Department will do all it can to get you up and running – quickly.

If you purchased your board from a Distributor:
Our distributors are technically capable and will help you to determine and correct your problem. Since your proof of purchase was obtained from the Distributor, please return your board to them. Please follow their instructions for returning your board for service.

If you purchased your board directly from Megatel:
Please Call or Fax to Megatel's Service Department prior to shipping, to receive your RMA# (Return Materials Authorization number). You may also submit a request for an RMA# from our web-site (http://www.megatel.ca). Boards that do not have RMA#s will not receive priority. To receive an RMA#, you will be required to provide the following information:

1. Company Name
2. Board Model Number or Product Order Number
3. Board Serial Number
4. Description of the Problem
5. Purchase Order Number

Special Shipping Instructions
Along with the information on the Megatel SERVICE FORM (see next page), please include the following on one of your commercial invoices:

1. The value of the board(s) – this value must match the invoice(s) we sent with the boards
2. A copy of the invoice(s) we sent with the boards (Proof of Purchase)
3. Be sure to state one of the following
   a) "Canadian Goods Being Returned for Repair"
   b) "Canadian Goods Being Returned for Warranty Repair"
   c) "Canadian Goods Being Returned"

One copy of the above documents is to be placed inside the shipping box and one copy is to be placed on the outside of the shipping box (marked for CUSTOMS). Other products (i.e. disk drives, LCD panels, etc.) that were not purchased from Megatel, but will be used as part of the servicing of the returned board, must be shipped separately and listed in the Megatel SERVICE FORM (next page) under "Equipment Sent Separately" heading. Products not purchased from Megatel should be shipped under a temporary import license of the maximum time limit.

Send PREPAID to the SERVICE DEPT. at:

MEGATEL COMPUTER CORPORATION
125 WENDELL AVENUE
WESTON, ONTARIO
M9N 3K9 CANADA

Our harmonized Number: 8471.92.00

Call us at +1 416 245-2953 between the hours of 9am to 5pm EST or send a Fax to +1 416 245-6505.

Megatel SERVICE FORM

PRIOR TO SHIPPING: : Please call Megatel to receive your RMA#. Only boards sent with an RMA# will be given priority. This RMA# must appear on all paper work and be clearly marked on the outside of the shipping box.

RMA#: _____

Date Called: _____

Your Company Name: _____

Your Contact Name: _____

Your Company Address:

Ship To: _____ **Bill To:** _____

Your Telephone Number: _____ **Extension:** _____

Your Fax Number: _____ **Extension:** _____

Equipment You are Sending to Us: Pleasefill in the following as completely and accurately as possible

Product #	Serial #	Description of the Problem

Purchase Order Number for this Return _____

Equipment Sent Separately

Courier	Waybill#	Description (include Model#, Serial#)

Courier Company to be Used for Returning this Shipment: Please Circle or Check One

FEDEX	EMERY	UPS AIR	PUROLATOR	ALPHA	TRANS	BAISLEY

OTHER _____

Special Instructions/Comments You have for us: _____

11 PC/II+vxe Physical Specifications

The physical size of the PC/II+vxe is compliant with the Megatel 4x4Family Specification. The size is 3.937 x 3.937 inches (100.0 x 100.0 mm). In the diagram, all dimensions are in MILS (1/1000'ths of an INCH).

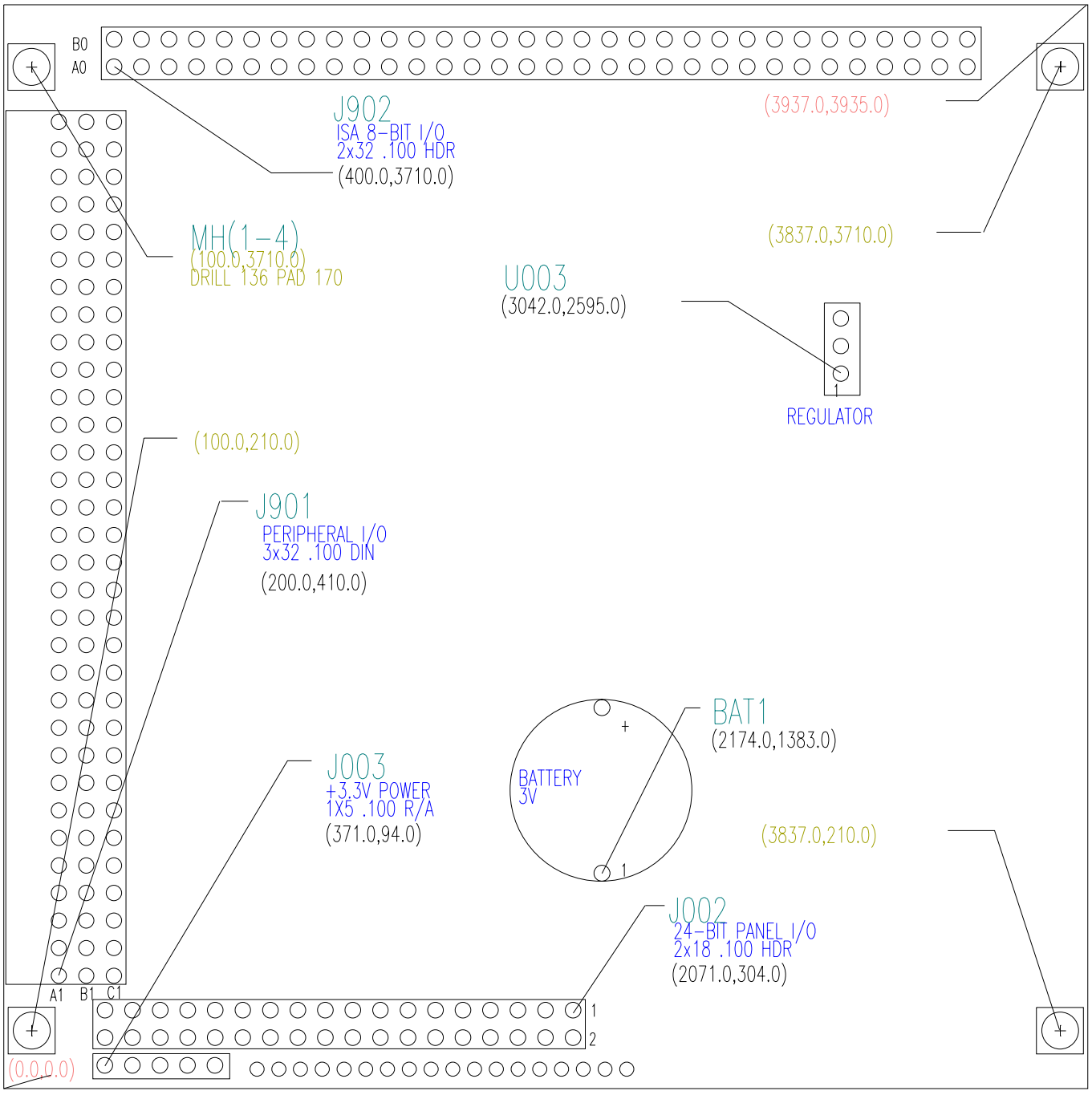


Figure 7 PC/II+vxe Physical Dimensions Diagram (v1.19)

12 PC/II+vxe Mechanical Isometric Drawing

An isometric drawing of the board (45°) illustrates the positioning of connectors (headers) on the top side of the board. The relative scale of all components with respect to the scale of the PCB has been maintained in the drawing.

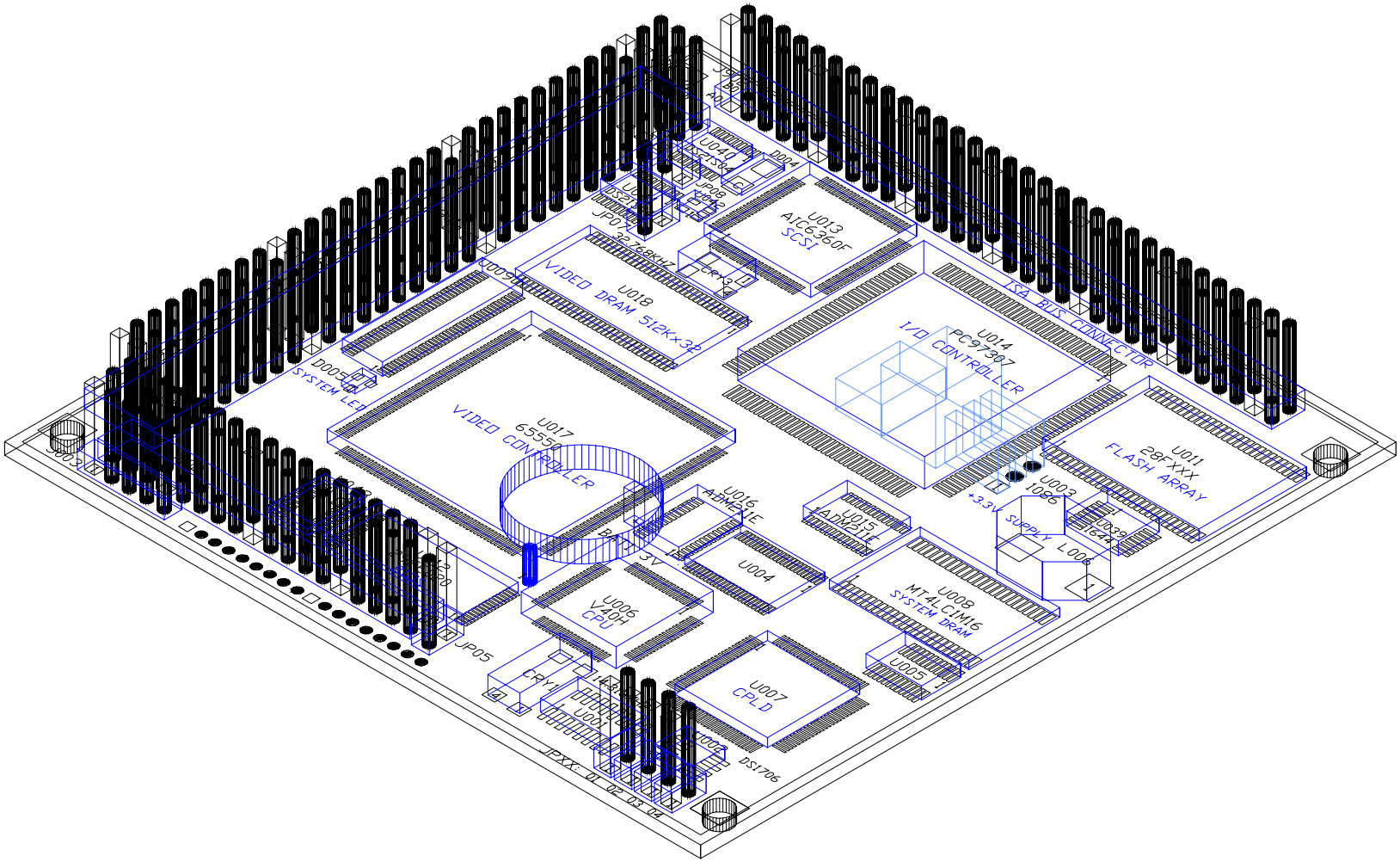


Figure 8 PC/II+vxe Mechanical Isometric Drawing (v1.19)