megatel

PC/II+dxe
Single-Board Embedded Computer

TECHNICAL REFERENCE Manual

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PC/II+dxe Single-Board Computer

megatel
4x4Family

PC/II+dxe Computer Cpu Board

The ***PC/II+dxe Computer Board*** is a rugged single-board computer with a full range of features that made us famous.

This board is available with a broad set of options that can be mixed in any combination to maximize price and performance. On-board options include DX4 or DX5 processors, Super VGA & LCD output, Ethernet, 2-8MB of soldered-down flash, a Flash Disk (Disk-on-Chip) socket, 4-32MB of soldered-down EDO DRAM, and IDE. Many other options and base features are packed into this tiny board, all of which are combined into a small and rugged, megatel 4x4Family compatible package with low power consumption.

Features

- megatel PC/II+dxe Board with Intel DX4 Write-Back Processor, or AMD DX4 Processor, or AMD DX5 Processor, and with ACC MICRO super I/O
- Supports 33 MHz Bus and 66, 100 or 133 MHz Cpu Clock
- 4 MB, 8 MB, 16 MB or 32 MB of soldered EDO DRAM memory
- 2MB, 4MB or 8MB of soldered flash array
- Flash disk socket (Disk-On-Chip) 2-144MB
- ISA 8-Bit Bus (and PC/104 connectivity)
- ISA 16-Bit Extension Option
- Megatel 4x4Family-compatible 96-pin I/O Interface uses Eurocard (DIN) Connector System
- Crystal CS8900 Ethernet 10Base-T and AUI Controller and Transformers & Filters
- ATA/IDE Hard drive interface
- AT compatible Keyboard interface
- On-board Mouse header
- Intel (Chips & Tech) 65550 CRT and Flat Panel Controller supports both CRT and Flat Panels
- On-board 36-pin LCD header extends direct I/O to panels to full 24-bits
- Supports 5V, or 3.3V Panels and CRTs
- Dual 8-Wire Serial Channels and a 2-Wire Serial Channel support full RS-232 communications
- Parallel Port ECP/EPP 1284 compliant
- Floppy Interface, Watchdog, RTC and all basic AT peripherals

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REVISION MT002401a 1999/0527
Prerelease Version for PC/II+dxe v1.00

REVISION MT002410a 1999/08/30
Release Version for PC/II+dxe v1.11

Document numbers in revision list updated & on title page	4
Bill of Materials and Component Placement diagrams updated	28, 30, 31
Physical Dimensions diagram added	109
Ordering Information Updated	99

REVISION MT002420 1999/10/04
Release Version for PC/II+dxe v2.00

Document numbers in revision list and notices updated & on title page	4
Added third serial option, COM4, a 2-Wire RS-232 Serial I/O Channel	3, 11-13, 15, 16-18, 28, 43-44, 60, 62-68, 70, 100-103, 109
Use of 128 KB flash for BIOS (in addition to 256 KB flash for BIOS) added	36
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REVISION MT002421 1999/11/19
Release Version for PC/II+dxe v2.03

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Physical Dimensions diagram updated	109
Cache control description expanded to clarify Write-back & Write-through (from Intel)	20,32
Bill of Material (major component) updated	28
Alternate +3.3V Power Connector (J3) added	33,33,66
Connector reference names changed to conform with component placement diagrams	Various
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Power Arrangement description (under Electrical Specifications) updated for dual supply	25
Absolute Maximum Ratings updated	25
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DC Characteristics updated	q
Support for 3.3V panels (in addition to 5V panels) added	46,Various

REVISION MT002422 1999/12/01
Release Version for PC/II+dxe v2.04

There were no significant changes to the layout or physical dimensions of the PCB.
This is a maintenance release only.

Component Top View diagram updated	30
Component Bottom View diagram updated	31
Physical Dimensions diagram updated	109
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Peripheral I/O Signal Summary updated	16
Recommended Operating Conditions updated	25
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Option L, 96-pin I/O & ISA Connector System, updated; Options x & y removed	104
Option c, Watchdog, updated	102
Table 12 updated, pin numbers corrected	50
References to Mouse clarified	Various
Block Diagram updated	18

REVISION MT002423 2000/01/12
Release Version for PC/II+dxe v2.05

There were no significant changes to the layout or physical dimensions of the PCB.

Component Top View diagram updated	30
Component Bottom View diagram updated	31
Physical Dimensions diagram updated	109
Bill of Material (major component) updated	28
DC Characteristics updated	26
COM4 description updated	44

CRT frequency supported to 80 MHz with Video at +3.3V	46ff

REVISION MT002424 2000/02/02

Release Version for PC/II+dxe v2.06

There were no significant changes to the layout or physical dimensions of the PCB.

Component Top View diagram updated	30
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Physical Dimensions diagram updated	109
Manufacturing Settings for Video were added (+5V and +3.3V options)	20ff
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Model number format updated	99ff
Component naming updated	Various

REVISION MT002425 2000/06/01

Release Version for PC/II+dxe v2.07

There were no significant changes to the layout or physical dimensions of the PCB.

Jumper JP03, JP01, JP05 were repositioned slightly	30,31
Component Top View diagram updated	30
Component Bottom View diagram updated	31
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ENAVEE panel signal can now be selected as active low or active high	46,20,64,103,104
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REVISION MT002426 2000/10/05

Release Version for PC/II+dxe v2.08

Production Release of PCB - no significant changes were made to v2.08 of the PCB

REVISION MT002428 2001/03/11

Release Version for PC/II+dxe v2.10

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1 Introduction

Welcome to the Megatel ***PC/II+dxe*** Cpu board, one of the Megatel ***4x4Family*** Cpu boards from Megatel Computer Corporation. In this document, you will find specifications for the functional, electrical, physical and operating characteristics of the PC/II+dxe Cpu board. Please feel free to contact Megatel or one of its distributors or agents if you require more information.

We have organized this document to present reference material, quick specifications, board settings and electrical specifications. The functional specifications begin in section 7, in topical order, including an introductory parts list and component placement diagrams. We conclude this document with resource maps, connector pinouts and signals, ordering and servicing information. Physical board specifications are placed at the end of the document.

1.1 PC/II+dxe Overview

PC/II+dxe is a fully functional single board computer which is Megatel 4x4Family compliant in its form factor and electrical interfaces. As a member of the Megatel 4x4Family, it is interchangeable with other members of the family to provide the feature set and performance range you require. The PC/II+dxe provides on-board 8-Bit or 16-Bit ISA bus connectors and 96-pin Eurocard (DIN) I/O connector to allow direct drop-in compatibility with existing and new designs.

PC/II+dxe contains a DX4 or DX5 processor and the processor can be shipped with a core operating frequency of 33 MHz, 50 MHz, 66 MHz, 100 MHz or 133 MHz. A maximum bus frequency of 33 MHz is supported on the 32-bit local bus by the PC/II+dxe. Typical processors shipped with the PC/II+dxe include the Intel 486DX4WB (33 MHz, 50 MHz, 66 MHz or 100 MHz), the AMD 486DX4 (100 MHz) or the AMD 486DX5 (133 MHz). Other compatible processors may also be ordered. Write-back class processors include an integrated write-back L1 cache. An ACC Micro 2089 Chipset provides an ISA Bus bridge, a DRAM memory controller, and a set of standard AT I/O peripherals. The board supports soldered-down DRAM EDO main memory (4 MB to 32 MB). An onboard CPLD supports the basic functionality of the board.

PC/II+dxe also contains a on-board Flash Bios and a 100% AT compatible bios. The board contains an optional soldered-down flash array with 2, 4 or 8 MB capacity.

A rich complement of peripheral controllers and interfaces is included. Full video is provided by the Chips & Tech 65550 controller, supporting CRT (R, G, B, Hsync, Vsync) or a wide variety of 4-bit (mono), 8-bit, 9/12-bit, 16-bit (double clocked) or (via optional LCD header) 24-Bit flat panels. Panels and CRT sync interfaces can be ordered to support either 5V or 3.3V interfaces. IDE, Keyboard, mouse (PS/2), and Floppy are provided by the ACC Micro 2089 bus controller. A full ECP/EPP Parallel port and two full serial ports are provided by the ACC Micro 2089 controller, and a two-wire RS-232 channel is also provided (and is used with BIOS calls); and the board also contains RS232 transceivers for all standard RS232 signals on all serial ports.

Peripheral I/O is pulled to a 96-pin DIN connector, that interfaces with Video CRT, 8-Bit or 16-bit Panels, Keyboard, 2 full Serial RS-232 ports, a two-wire RS-232 serial port and a full Parallel port. In addition to the compatible DIN connector interface to video CRT and Panels, the board also provides an on-board 36-pin header to support the full 65550 controller panel interface. An on-board 2-pin header can be interfaced to a PS/2 mouse. The Ethernet interfaces are provided separately on a standard 2X5 pin header. IDE is provided by an on-board 44 pin 2mm header. A 12-pin power header is provided to supply the single +5V rail to the board and the +5V rail is regulated to +3.3V on the board.

The Megatel 4x4Family PC/II+dxe has been designed for rugged and reliable operation in a low-cost compatible package, and extends the Megatel 4x4Family product line. The board is offered in its base configuration that consists of minimal memory, system controller and CPU. Any combination of peripherals can be populated at your option to meet your price/performance requirements.

2 Reference Documents

2.1 Datasheets

ACC Micro	ACC2089 Enhanced Super Chip, Databook, 1997
AMD	Enhanced Am486®DX Microprocessor Family, 20736 Rev B Amendment/0, Mar 1997
Analog Devices	EMI/EMC Compliant ±15 kV ESD Protected RS-232 Line Drivers/Receivers (ADM211E), 1996
Intel (Chips and Tech)	65550 (HiQV32™) High Performance Multi-Media Flat Panel / CRT GUI Accelerator, Revision 1.5, Dec 1997 65550 HiQVideo Series Mode Support, 020089-004 (AN89.4), Revision 1.4, Feb 1996
Crystal Semiconductor Corp	CS8900 Highly Integrated Ethernet Controller, DS150PP2, Dec 95
Dallas Semiconductor	DS1706S 3.3V and 5.0V MicroMonitor, Feb 1998
Dallas Semiconductor	DS1685 Real Time Clock, Mar 1998
Intel	Embedded Write-Back Enhanced IntelDX4™ Processor, 272771-002, Dec 1997
Intel	Embedded Intel486™ Processor Family Developer's Manual, 273021
Intel	Embedded Intel486™ Processor Hardware Reference Manual, 273025
Intel	Intel486 Microprocessor Family Programmer's Reference Manual, 240486
Intel	INTEL® StrataFlash™ Memory Technology 32 and 64 Mbits (28F640J5), 290606-006, Jul 1998
Valor Electronics Inc.	ST7010 10Base-T Transformer Datasheet, Rev C
Valor Electronics Inc.	Ethernet AUI Transformers (ST7033) Datasheet, E/AUI105-01, Nov 1995

2.2 Reference Standards

Annabooks	AT Bus Design IEEE P996-Compatible, Edward Solari
IEEE	P996.1 Standard for Compact Embedded-PC Modules

2.3 Other References

Megatel	Ethernet Appbook, MT0047-02
Microsoft Press	The Programmer's PC Sourcebook, Thom Hogan

3 Specification Summary

3.1 PC/II+dxe Board Specifications

Board Form Factor:	3.937 x 3.937 inch (100.0 x 100.0 mm)
Board Type:	FR4
Basic Board Requires:	Central Processing Unit Minimum Memory – Soldered, 4 MB Minimum Connectors – Power and I/O as Needed
Architecture:	PC/AT
Central Processing Unit:	486DX4 RISC-Core Processor – Intel or AMD INTEL DX4: 66 MHz or 100 MHz core speed with 33 MHz local bus speed, or 50 MHz or 33 MHz core speed with 16 MHz local bus speed 3.3V core and 5V tolerant I/O 32-Bit RISC technology core Pipelined execution Integrated Floating-Point unit Integrated Write-Back or Write-Through Cache AMD DX5: 133 MHz core speed with 33 MHz local bus speed 3.3V core and 5V tolerant I/O 105.6 million bytes/second burst bus 0.35-u CMOS-process technology Integrated Floating-Point unit Integrated Write-Back or Write-Through Cache
Cache Memory:	16K of integrated on-chip Cache Memory (L1) Unified organization, uses modified MESI protocol High performance write-back and write-through (user options)
DMA:	(7) Channels, 128 MB addressing
Timer/Counters:	AT-compatible
PC Speaker Output:	Available on Peripheral I/O connector
Memory Bus:	32-Bit
Address Bus:	32-Bit
Power Monitoring:	Dual 5% monitor – 5V rail and on-board 3.3V Reset hold time – 130 ms minimum, 200 ms typical Transient voltage immunity
Manual Reset:	Available on 96-pin DIN I/O Connector Generates minimum of 130ms reset on Low to High Initiated by pulling Manual Reset signal line Low, then High TTL (+5V to 0V) tolerant

Memory:	DRAM EDO (soldered) memory Minimum System Memory 4 MB Maximum System Memory 32 MB DRAM – EDO, 60 ns typical
Memory Options:	4, 8, 16 or 32 MB
Keyboard:	PS/2-style Keyboard supported by 96-pin DIN interface
Mouse:	PS/2-style Mouse supported by on-board 2-pin Header
Printer/Parallel Port:	Full Bi-directional ECP/EPP Parallel Port supported
Serial/RS232 Ports:	(1) or (2) 16C550-compatible Serial Ports 16-byte FIFOs Full EIA-RS232E and CCITT V.28 Transceivers included Output swing ±9V with all Transmitter Outputs loaded with 3K ohms to Ground
Two-Wire Serial RS-232:	(1) BIOS-accessible RS-232 two-wire (Rxd & Txd) Serial Port Full EIA-RS232E and CCITT V.28 Driver & Receiver included Output swing ±9V with all Transmitter Outputs loaded with 3K ohms to Ground
Video CRT & Flat Panel:	Chips and Technologies HiQ 65550 GUI Accelerator On-board 2 MB of 60 ns Video EDO DRAM, 512Kx32 Complete Analog CRT Video Interface Complete 24-Bit Flat Panel Interface provided by on-board 36-pin Header Compatible 8-Bit or 16-Bit Panel Interface also provided on 96-Pin DIN Connector Monochrome (64 gray scale) or color Hi-Res Passive STN, Active Matrix TFT/MIM LCD, EL Simultaneous CRT / Flat Panel operation supported using on-board 36-pin interface Header Local bus interface – 32-Bit 64-bit Graphics Accelerator engine (BitBLT), H/W cursor VGA register set compatibility Supports 5V and 3.3V panels from popular manufacturers such as Sharp, Optrex, Toshiba, Hitachi, Fujitsu, Samsung, NEC, Sanyo and others Chips and Technologies drivers included
ATA/IDE Hard Drives:	(2) IDE drives supported
ISA Bus:	2x32 8-Bit ISA bus Interface Header 1x10 16-Bit ISA bus Interface Extension Header
Flash Array: **Flash Disk:**	Soldered Flash EEPROM – 2, 4 or 8 MB Socket for user-supplied M-Systems Disk-on-Chip solid-state disk Support for MD2000 modules (2 to 144MB capacity) Coexistence support for both Flash Array and Flash Disk
Ethernet:	Crystal CS8900 High-performance 10Base-T and AUI controller option IEEE 802.3 compliant MAC engine, full duplex operation On-chip RAM buffers – for Transmit & Receive frames

AUI port for 10Base-2, 10Base-5 and 10Base-F
10Base-T filters included
10Base-T and AUI isolation transformers are included
10Base-T port has automatic polarity detection and correction
Auto negotiation function
LED for inbound/outbound frames to/from local controller included
LED for either valid 10Base-T link present, or other general function

Floppy Disk:

Integrated Floppy Disk Controller
(2) 3.5" floppy disk drives supported
IBM System 34 double density format (MFM)
Sony EMCA format compatible
Standard transfer rates – 500 Kb/sec, 300 Kb/sec and 250 Kb/sec

Real-Time Clock, Alarm:

Dallas-Certified DS1685 – Y2K Real-Time Clock Controller
Periodic Interrupt Generator – settable to period from 122 us to 500 ms
Alarm Interrupt Generator – settable to any time of day in 24 hour period
242-byte NVRAM included
12 or 24 hour format
Daylight savings time support
Unique 48-Bit Serial Number can be used for customer application

Watchdog:

Dallas DS1706 Watchdog Timer/Monitor
Defaults at power-on time to software-disabled state
Software enable/disable/strobe is supported
Minimum strobe rate while enabled – 1 strobe/second
Hardware enable/disable jumper option

Connectors:

+5V Power Connector –
    +5V Power supplied to Board through 96-pin DIN Connector
    Optional 1x12 R/A +5V keyed Power Header, 15A rating
+3.3V Power Connector –
    +3.3V Power generated by on-board regulator
    Optional 1x5 R/A +3.3V Power Header, keyed, 6A rating
I/O Interface Connector –
    (1) 3x32 (.100 inch pitch) Right-Angle Connector
    Support top mounting (bottom by request)
    Support standard headers on request
      (including board stacking headers)
ISA-bus Connectors –
    (1) 2x32 and (1) 1x10 pin and socket header
    stack-through and non stack-through
    board stacking is customer specified
Ethernet Header –
    (1) 2x5 header
IDE Header –
    (1) 2x22 2mm Header
FULL VIDEO Header –
    (1) 2x18 Header
    Support full 24-bit panels
    Support either 5V or 3.3V panels
    Support Simultaneous Video CRT and Panel Modes
All connectors are optional, except one of the I/O Interface
    connector or the +5V Power connector must be present

Peripheral I/O Signals:	Signal Pins – 96-Pin DIN Interface Connector Video CRT & Panel – 17 PC Speaker – 1 Parallel (LPT1) I/O – 17 SCSI – 18 Serial COM1 (RS-232E) – 8 Serial COM2 (RS-232E) – 8 Serial COM4 (RS-232) – 2 Keyboard – 2 Floppy – 15 Reset Switch – 1 Power & Ground Signal Pins – Other I/O Headers Video Panel (Extended 36-pin Header) – 32 Ethernet 10-pin Header – 10 IDE 44-pin Header – 28 Mouse Header – 2
System LED:	On-board system LED confirms Bios & Hardware status
Supply Voltage:	Single supply at +5V 5%, or Dual Supplies at +5V 5% and +3.3v 5%
Supply Power Rating:	5W to 15W (excluding external peripheral requirements)
Supply Regulation:	+5V (and optional +3.3V Supply) require regulation to within 5%
Supply Rise Time:	+5V Supply maximum rise time (+3V to +5V) required within 100 ms +3.3V Supply maximum rise time (+3V to +5V) required within 100 ms
Supply Regulators:	Optional On-board +5V to +3.3V Switching or Linear Regulator On-board power monitor for both +5V and +3.3V rails
Storage Temperature:	-50C to +125C, battery excluded
Operating Temperature:	Commerical 0C to +70C standard Industrial -20C to +85C available on request Industrial -40C to +85C available on request
Operating Software:	DOS, Windows, Windows 95, Windows NT4.0
Application Software:	x86 compatible
Bios Software:	256 KB Flash EEPROM for Bios Bios write protection (hardware) Chips & Technologies 65550 VGA Driver BIOS included AT compatible BIOS and Architecture

3.2 PC/II+dxe Board Block Diagram

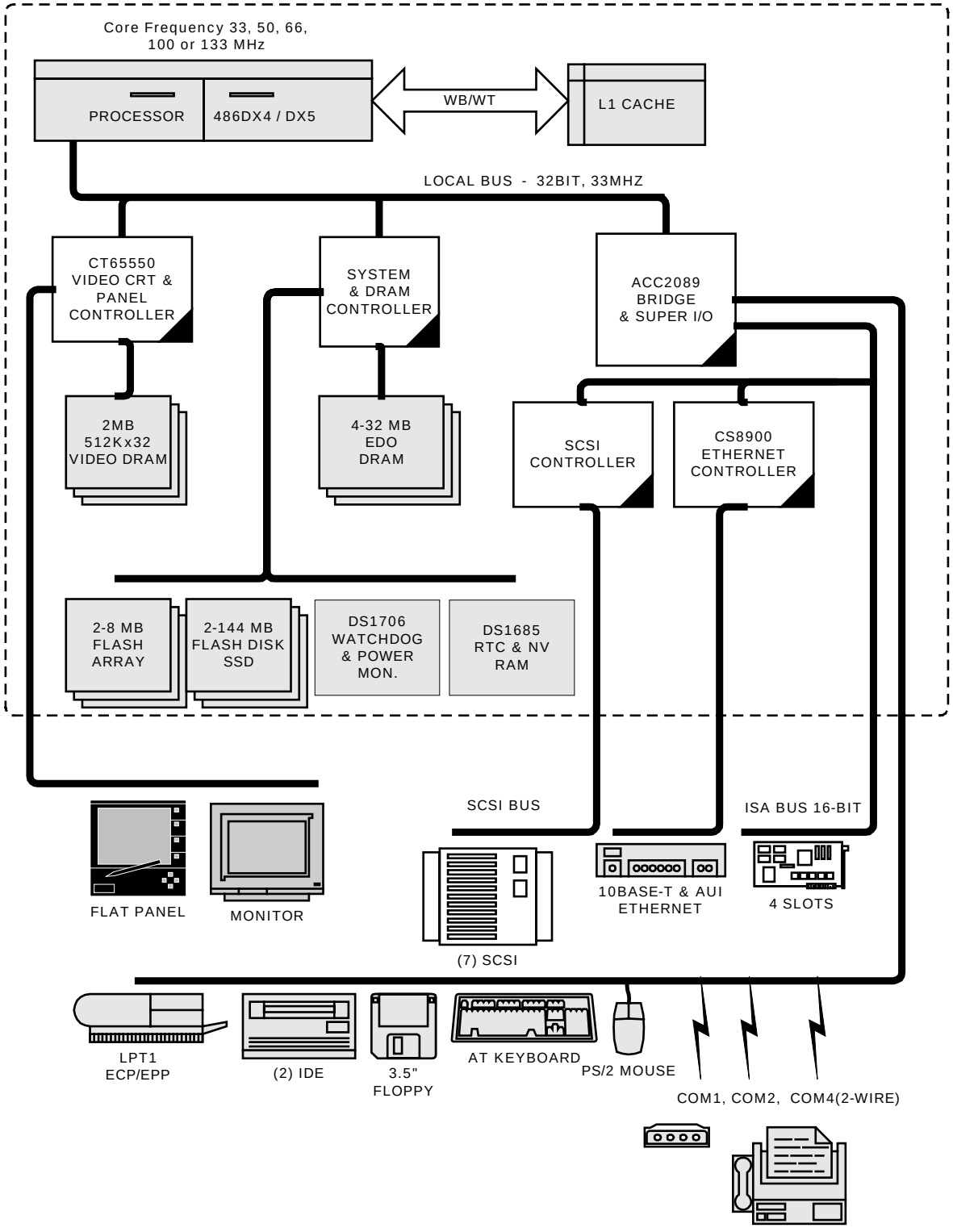


Figure 1 PC/II+dxe Block Diagram (v2.10)

4 Settings

4.1 Jumper Settings

Refer to the PC/II+dxe Component Placement diagram. All jumpers are on the TOP side of the board.

Table 1 Jumper Settings

JUMPER	SETTING	SELECTED OPTION	COMMENT
JP01	open	Watchdog disabled	The watchdog cannot be operated.
	closed	Watchdog enabled	The watchdog controller and its internal functionality will always operate, whether or not this jumper is installed. However, the system will ONLY be forced into reset state if, at the time of a watchdog timer expiry, the watchdog is enabled by software, the timer has expired and this jumper is INSTALLED.
JP02	open	Normal operation	
	closed	Reset RTC CMOS memory	This function is required to be enabled by the BIOS. Before closing (installing) this jumper, VCC Power may be present or not present. When the jumper is installed and the function has been enabled by the BIOS, the contents of the RTC NV SRAM User memory (242 bytes used for system configuration) is cleared. The jumper is required to be removed before power is applied (if power is applied when the jumper is installed, remove the jumper and then cycle the power to restore operation). On reboot, default configuration parameters are restored by the BIOS.
JP03	open	External bios	Used by Megatel manufacturing only
	closed	Normal operation	(default) Jumper must be present for normal operation.
JP04	open	Normal operation	(default)
	closed	Program bios	Used by Megatel manufacturing only

4.2 Manufacturing Settings

Except for jumper settings, all features and options on the board are factory installed (for a complete list of manufacture and feature options, see section 0 on page 99).

In the following tables, certain manufacturing features or options are described in more detail to assist you in selecting which setting to order. For more information, please contact your distributor or agent, or contact Megatel directly if you have specific questions or manufacturing requirements.

Table 2 Manufacturing Settings

ORDER OPTION	SETTING	SELECTED OPTION	COMMENT
Option "a" (page 101)	0	Write-Back	(default) L1 Cache operates in Write-Back Mode; Intel documentation states: “This type of cache-control provides the best performance, but it requires that all devices that access system memory on the system bus be able to snoop memory accesses to insure system memory and cache coherency.” All on-board devices conform to this requirement, and provided that user bus devices conform, this setting is recommended to provide the **highest CPU performance**.
	1	Write-Through	L1 Cache operates in Write-Through Mode; Intel documentation states: “This type of cache-control is appropriate for frame buffers or when there are devices on the system bus that access system memory, but do not perform snooping of memory accesses. It enforces coherency between caches in the processors and system memory.” Use of this setting safely provides cache coherency no matter what user bus devices are present. See Write-Back.
Option "b" (page 101)	0	SCSI is Primary	(default) SCSI controller is primary device, I-O base is at 340h; this option also applies when SCSI is not configured on a board
	1	SCSI is Secondary	SCSI controller is secondary device, I-O base is at 140h; using this option allows another SCSI controller to be used from the ISA bus which is configured as a primary controller

ORDER OPTION	SETTING	SELECTED OPTION	COMMENT
Option "c" (page 102)	0	Watchdog Not Installed	(default) Watchdog is hardware disabled and cannot be operated. The board is shipped without the disable/enable jumper installed (JP01)
	1	Watchdog Installed but is H/W Disabled	Watchdog Jumper is installed, but a jumper socket is not installed. Therefore, in this state the board cannot operate with the watchdog. The watchdog can be placed into operating mode in the field by (a) installing a jumper socket on JP01, and (b) enabling the watchdog using the appropriate BIOS function call.
	2	Watchdog Installed, H/W Enabled, but S/W Disabled	Watchdog is installed and ready to use by the Software. The BIOS disables the watchdog by default at boot time, and the watchdog can be enabled by calling the appropriate software BIOS function.
Option "d" (page 102)	0	IDE Cable Select NOT Grounded at Host	(default) IDE Cable Select signal (CSEL, pin 28) is not grounded on the host PC/II+dxe board; this option allows the customer to use this signal as SPSYNC (see ATA standard), or to provide device selection off-board
	1	IDE Cable Select IS Grounded at Host	The CSEL signal on the IDE bus (pin 28 on the IDE header) is tied to ground on the PC/II+dxe board for use in device selection using the Cable Select method of selection
Option "e" (page 102)	0	ISA IRQ10 is IRQ10	(default) ISA IRQ10 is tied to interrupt controller IRQ10
	1	ISA IRQ10 is IRQ15	ISA IRQ10 is tied to interrupt controller IRQ15
Option "f" (page 103)	0	ISA DACK16# is DACK7# and DACK6#	(default) ISA DACK16# is driven by the logical AND of DACK7# and DACK6#
	1	ISA DACK16# is MASTER# and DACK6#	ISA DACK16# is tied to the logical AND of MASTER# and DACK6#
Option "g" (page 103)	0	ISA IRQ14 is IRQ14	(default) ISA IRQ14 is tied to interrupt controller IRQ14
	1	ISA IRQ14 is DRQ7	ISA IRQ14 is tied to DREQ7 (DMA channel 7)
	2	ISA IRQ14 is DRQ6	ISA IRQ14 is tied to DREQ6 (DMA channel 6)

ORDER OPTION	SETTING	SELECTED OPTION	COMMENT
Option "h" (page 103)	0	Panel Type on DIN 96-pin Connector is Monochrome SS 8-Bit	Monochrome SS 8-Bit Panels are supported through the 96-pin DIN Connector. The 96-pin panel interface pins are mapped to the 65550 video controller pins as follows: DIN.B2 (P0) is tied to 65550.P8 DIN.B3 (P1) is tied to 65550.P9 DIN.B4 (P2) is tied to 65550.P10 DIN.A1 (P3) is tied to 65550.P11 DIN.C5 (P4) is tied to 65550.P12 DIN.A2 (P5) is tied to 65550.P13 DIN.B6 (P6) is tied to 65550.P14 DIN.C6 (P7) is tied to 65550.P15 DIN.A4 (SCK) is tied to 65550.SHFCLK DIN.C3 (LC) is tied to 65550.LP/DE/BLANK# DIN.C2 (FRM) is tied to 65550.YD/FLM DIN.A5 (M) is tied to 65550.M/DE/BLANK#
	1	Panel Type on DIN 96-pin Connector is Color TFT 9/12-Bit	Color TFT 9 or 12-Bit Panels are supported through the 96-pin DIN Connector. The 96-pin panel interface pins are mapped to the 65550 video controller pins as follows: DIN.B2 (P0) is tied to 65550.P1 DIN.B3 (P1) is tied to 65550.P2 DIN.B4 (P2) is tied to 65550.P3 DIN.A1 (P3) is tied to 65550.P4 DIN.C5 (P4) is tied to 65550.P7 DIN.A2 (P5) is tied to 65550.P8 DIN.B6 (P6) is tied to 65550.P9 DIN.C6 (P7) is tied to 65550.P10 DIN.A3 (P8) is tied to 65550.P12 DIN.C4 (P9) is tied to 65550.P13 DIN.A6 (P10) is tied to 65550.P14 DIN.A7 (P11) is tied to 65550.P15 DIN.A4 (SCK) is tied to 65550.SHFCLK DIN.C3 (LC) is tied to 65550.LP/DE/BLANK# DIN.C2 (FRM) is tied to 65550.YD/FLM DIN.A5 (M) is tied to 65550.M/DE/BLANK#
	2	Panel Type on DIN 96-pin Connector is Color STN Ext 4-Bit Packed	Color STN Extended 4-Bit Packed panels are supported through the 96-pin DIN Connector. The 96-pin panel interface pins are mapped to the 65550 video controller pins as follows: DIN.B2 (P0) is tied to 65550.P0 DIN.B3 (P1) is tied to 65550.P1 DIN.B4 (P2) is tied to 65550.P2 DIN.A1 (P3) is tied to 65550.P3 DIN.C5 (P4) is tied to 65550.P4 DIN.A2 (P5) is tied to 65550.P5 DIN.B6 (P6) is tied to 65550.P6 DIN.C6 (P7) is tied to 65550.P7 DIN.A4 (SCK) is tied to 65550.SHFCLK DIN.C3 (LC) is tied to 65550.LP/DE/BLANK# DIN.C2 (FRM) is tied to 65550.YD/FLM DIN.A5 (M) is tied to 65550.M/DE/BLANK#

Option "j" (page 103)	0	DIN 96-pin Connector P8 is P12	DIN.A3 (P8) is tied to 65550.P12. Select this option if Option 9 = 2
	1	DIN 96-pin Connector P8 is ENAVEE	DIN.A3 (P8) is tied to 65550.ENAVEE; this signal is conditioned to be active low or active high - see option "n"
Option "k" (page 104)	0	DIN 96-pin Connector M is M	DIN.A5 (M) is tied to 65550.M
	1	DIN 96-pin Connector M is ENAVEE	DIN.A5 (M) is tied to 65550.ENAVEE; this signal is conditioned to be active low or active high - see option "n"
Option "n" (page 104)	0	ENAVEE is Active Low	The ENAVEE signal that will be output on connector pins J002.31, J901.A3 and J901.A5 will be Active Low; select this option if you will be using the compatible video interface on the 96-pin DIN connector.
	1	ENAVEE is Active High	The ENAVEE signal that will be output on connector pins J002.31, J901.A3 and J901.A5 will be Active High.

ORDER OPTION	SETTING	SELECTED OPTION	COMMENT
Option "r" (page 105)	1	SINGLE SUPPLY J901 (+5V) LINEAR P.S. (+3.3V)	(default) A single +5v supply is required; All +3.3v power is generated on-board using a linear power supply +5v is supplied to J901 (96-pin DIN connector).
	2	SINGLE SUPPLY J901 (+5V) SWITCH P.S.(+3.3V)	A single +5v supply is required; All +3.3v power is generated on-board using a switching power supply +5v is supplied to J901 (96-pin DIN connector).
	3	DUAL SUPPLY J901 (+5V) J003 (+3.3V)	Dual +5v and +3.3v supplies are required. There are no on-board power supplies. +5v is supplied to J901 (96-pin DIN connector) and +3.3v is supplied to J003 (5 pin header).
	4	SINGLE SUPPLY J906 (+5V) LINEAR P.S. (+3.3V)	A single +5v supply is required; All +3.3v power is generated on-board using a linear power supply +5v is supplied to J906 (12 pin header).
	5	SINGLE SUPPLY J906 (+5V) SWITCH P.S.(+3.3V)	A single +5v supply is required; All +3.3v power is generated on-board using a switching power supply +5v is supplied to J906 (12 pin header).
	6	DUAL SUPPLY J906 (+5V) J003 (+3.3V)	Dual +5v and +3.3v supplies are required. There are no on-board power supplies. +5v is supplied to J906 (12 pin header) and +3.3v is supplied to J003 (5 pin header).
Option "V" (page 106)	0	NO VIDEO	The Video controller and components associated with the controller and video interface are not populated.
	1	VIDEO AT +5V	The Video system components are populated. The video controller is configured to output a voltage swing of 5V to the LCD panel (all data lines and control lines) and to the CRT interface (HSYNC and VSYNC).
	2	VIDEO AT +3.3V	The Video system components are populated. The video controller is configured to output a voltage swing of 5V to the LCD panel (all data lines and control lines) and to the CRT interface (HSYNC and VSYNC).

5 Electrical Specifications

The PC/II+dxe board operates on a single +5V ± 5% supply, or on dual supplies of +5V ±5% and +3.3V ±5%. An on-board dual voltage monitor is used. When a single +5V supply is used, the PC/II+dxe board is shipped with an on-board regulator which generates the +3.3V.

The PC/II+dxe board is normally supplied with +5V from the 96-pin DIN connector (J901), and may alternatively be supplied with +5V using a separate +5V power header (J906) provided on the board. If dual supplies are to be used, a +3.3V power header (J003) may be ordered. Refer to section 10.3.20, page 105, for information on ordering the Power Supply Arrangement.

5.1 Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
Power Supply	Digital	VCC5	-0.3	6.0	V
		VCC3	-0.3	3.6	V
Ambient Temperature	**(Note 1)**	TA	-55	+125	°C
Storage Temperature	**(Note 1)**	TS	-65	+150	°C

Warning: ***Operation at or beyond these limits may result in permanent damage to the board or to components attached to the board. Always operate the board at the Recommended Operating Conditions, see below.***

Note 1. ***Temperature is given for a board for which power is NOT applied and a Battery is NOT included onboard. If the board contains a lithium battery, then the absolute temperature board ratings must be modified to meet the more restrictive ratings for lithium batteries. Refer to manufacturer's specifications for Lithium Batteries. Never exceed the ratings of a lithium battery if a battery is present on the board.***

5.2 Recommended Operating Conditions

Parameter		Symbol	Min	Typical	Max	Units
Power Supply	Digital	VCC5	4.75	5.0	5.25	V
		VCC3	3.14	3.3	3.46	V
Power Supply Rise Time	+3.0V to +5.0V	VCC5S			100	ms
Operating Ambient Temperature	**(Note 1)**	TA	0		70	°C
Storage Ambient Temperature	**(Note 1)**	TS	-55		+125	°C
Humidity	(Untested)	HA	10		90	% RH

Note 1. ***Temperature is given for a board for which power IS applied, but a Battery is NOT included. If the board contains a lithium battery, then the absolute temperature board ratings must be derated to meet the specifications for lithium batteries. Refer to manufacturer's specifications for Lithium Batteries. Never exceed the ratings of a lithium battery if a battery is present on the board.***

5.3 DC Characteristics

Over Recommended Operating Conditions

Parameter		Cpu Freq	Bus Freq	Symbol	Min	Typical	Max	Units	*Note*
Power Supply	(digital)	MHz	MHz	VCC	4.75	5.0	5.25	V	
Power Supply Current				ICC		950		mA	***1***
Power (+5V External, +3.3V Onboard Switching Supply)	DX4 - Intel	33	16	PDD		4.2		W	***1***
	DX4 - Intel	66	33	PDD		4.9		W	***1***
	DX4 - Intel	100	33	PDD		5.9		W	***1***
	DX5 - AMD	133	33	PDD		5.2		W	
	DX5 - AMD	66	16	PDD		4.1		W	
Power (+5V External, +3.3V External)	DX4 - Intel	66	33	PDD5		2.0		W	***2***
				PDD3		2.8		W	***2***

Note 1. ***Single Supply Configuration. INTEL DX4 CPU or AMD DX5 CPU operating at specified core frequency and specified local bus frequency, 16 MB of EDO DRAM installed, with Video installed and an attached VGA CRT, and a switching +3.3V regulator on-board.***

Note 2. ***Dual Supply Configuration. INTEL DX4 CPU operating at specified core frequency and specified local bus frequency, 16 MB of EDO DRAM installed, 2 MB Soldered Flash installed, SCSI installed, Ethernet installed, IDE installed, and with Video installed and an attached VGA CRT. Both +5V and +3.3V are externally supplied to board.***

5.4 Voltage Monitor

An on-board micro voltage monitor is included in the PC/II+dxe board. The Dallas Semiconductor DS1706S device provides both a watchdog function and a dual-voltage monitor function. The outputs of the device are directed to the system reset bus, RST and RST#, to provide a system reset at the time of a persistent power exception. The on-board generated +3.3V supply rail is monitored at minus 5% by the primary voltage monitor, and the +5V supply is monitored by the IN input voltage sense monitor, using a precision bridge to step the +5V down to the Input Trip Point (1.25V).

Over Recommended Operating Conditions

Parameter		Symbol	Min	Typical	Max	Units
+5V Supply Voltage		VCC5	4.75	5.0	5.25	V
+3.3V Supply Voltage	External Supply	VCC3	3.15	3.3	3.45	V
IN Input Trip Point		VTP	1.20	1.25	1.30	V
VCC3 Trip Point DS1706	(primary)	VCCTP	2.85	2.93	3.00	V
VCC5 Trip Point DS1706 (IN)	NOTE 1	VTP5	4.05	4.29	4.53	V
Reset Active Time		TRST	130	205	285	ms
VCC Detect to RST and RST#		TRFP	130	204	285	ms
PBRST# Stable Low to RST and RST#		TDLY			250	ms
VIN Detect to NMI#		TIPD		5	8	us

NOTES
1) The +5V supply to the board MUST be externally regulated to produce +5.0V on the board; and if +3.3V is externally supplied, the external supply must be externally regulated to produce +3.3V on the board.

5.5 Bus Drive Current

Most ISA bus signals have a reduced bus drive requirement of 4 mA. The 4 exceptions are open collector driven signals, which must drive 330-ohm pullup resistors defined by the P996 specification.

The following signals must be driven with devices capable of providing 20 mA sink current:

MEMCS16#, IOCS16#, MASTER# and ENDXFR#.

All other signals may be driven with devices capable of providing 4 mA sink current.

6 Component Information

6.1 Bill of Material

The major components on the PC/II+dxe board are contained in the following table. See Notes.

Table 3 Board Component List (v2.10)

REF	QTY	DESCRIPTION [1]	PART [2]	VENDOR
BAT1	1	BATTERY – 3.0V Lithium		
C125	1	CAPACITOR – 100 uF 6V TANTALUM		
CRY1	1	CRYSTAL – 14.31818 MHz		
CRY2	1	CRYSTAL – 32.768 KHz		
D002	1	LED – Dual, Ethernet Line & Local Activity		
D004	1	LED – Single, System Status		
F001	1	TRANSFORMER – Isolation, Ethernet 10Base-T	ST7010T	VALOR
F002	1	TRANSFORMER – Isolation, Ethernet AUI	ST7033	VALOR
J001	1	HEADER – CPU FAN +5V & GND – 1x2 1.25 mm	53057-0210	MOLEX
J002	1	CONNECTOR – PANEL 24-BIT, 2X18 .100		
J003	1	CONNECTOR – POWER +3.3V, 1X5 .100 Right-Angle Header		
J901	1	CONNECTOR – DIN R/A, 3x32 .100		
J902	1	CONNECTOR – ISA BUS 8-BIT, 2X32 .100 Header		
J903	1	CONNECTOR – ETHERNET, 2X5 .100 Header		
J904	1	CONNECTOR – IDE/ATA, 2x22 2mm Header		
J905	1	CONNECTOR – ISA BUS 16-BIT EXTENSION, 1X10 .100 Header		
J906	1	CONNECTOR – POWER +5V, 1x12 .100 Right-Angle Header	22-05-2121	MOLEX
JP01,JP02 JP03,JP04	4	JUMPER – 1x2 .100	M20-9990206	HARWIN
JP05	1	HEADER – MOUSE, 1X2 .100	M20-9990206	HARWIN
L006	1	INDUCTOR – 6.8 uH		
U001	1	CONTROLLER – Bus & DRAM Controller & Super I/O	ACC2089	ACCMICRO
U002,U003 U006,U007	4	DRAM – EDO, 2MB Memory, 50 ns typical	MICRON	MT4LC4M16
U008	1	LOGIC – Gate		
U009	1	LOGIC – Bus Logic	2016	
U010	1	REGULATOR – Voltage Regulator	LT108X-3.3	LINEAR
U011	1	MONITOR – Power Monitor & Watchdog Controller	DS1706	DALLAS
U012	1	REGULATOR – Voltage Regulator (Alternate position for U10)		
U013	1	PROCESSOR – Processor, 100 MHz or 133 MHz	AM486DX5	AMD
	1	PROCESSOR – Processor, 66 MHz or 100 MHz	FX80486DX4	INTEL
U016	1	CPLD		
U021	1	FLASH ROM – ARRAY, 16 Mbit (2MB) Flash	28F160	INTEL
	1	FLASH ROM – ARRAY, 32 Mbit (4MB) Flash	28F320	INTEL
	1	FLASH ROM – ARRAY, 64 Mbit (8MB) Flash	28F640	INTEL
U025	1	FLASH ROM – BIOS, 2 Mbit (256KB) Flash	29EE020	SST
U028,U029	2	TRANSCEIVER – RS232E Transceivers	ADM211E	ANALOG
U033	1	SCSI Controller		
U034	1	ETHERNET – Ethernet Controller	CS8900	CRYSTAL

REF	QTY	DESCRIPTION [1]	PART [2]	VENDOR
U035	1	ETHERNET – Configuration EEPROM	92C46	
U036	1	VIDEO – Video CRT/Flat Panel Controller	65550	CHIPS
U037	1	DRAM – VIDEO, EDO, 2MB Memory, 512Kx32		
U038	1	LOGIC – Gate		
U039	1	LOGIC – Gate		
U040	1	DISC-ON-CHIP SOCKET – for user-supplied Flash Disk Module		
U041	1	CLOCK – Quad Programmable Clock Generator		
U042	1	LOGIC – Gate		
U043	1	RTC – Real-Time Clock	DS1685	DALLAS
U044	1	LOGIC – Gate		
U047	1	LOGIC – Gate		
U048	1	LOGIC – Gate x 4		
U049	1	LOGIC – Multiplexor		
U051	1	REGULATOR – SWITCHING 5V TO +3.3V – OPTIONAL		

NOTES

[1] For component specifications, refer to the applicable data sheets from the component respective manufacturer.

[2] All part numbers are generic, and boards may be shipped with alternatively-sourced parts which are functionally equivalent. ***If substitution of parts is required by Megatel, Megatel will make every attempt to provide a functionally equivalent parts, and Megatel reserves the right to change any component on the board. Please contact your distributor or agent, or contact Megatel directly if you have specific component requirements****.*

6.2 Component Placement – Top Side

The following diagram shows the major components on the top (component) side of the PC/II+dxe board.

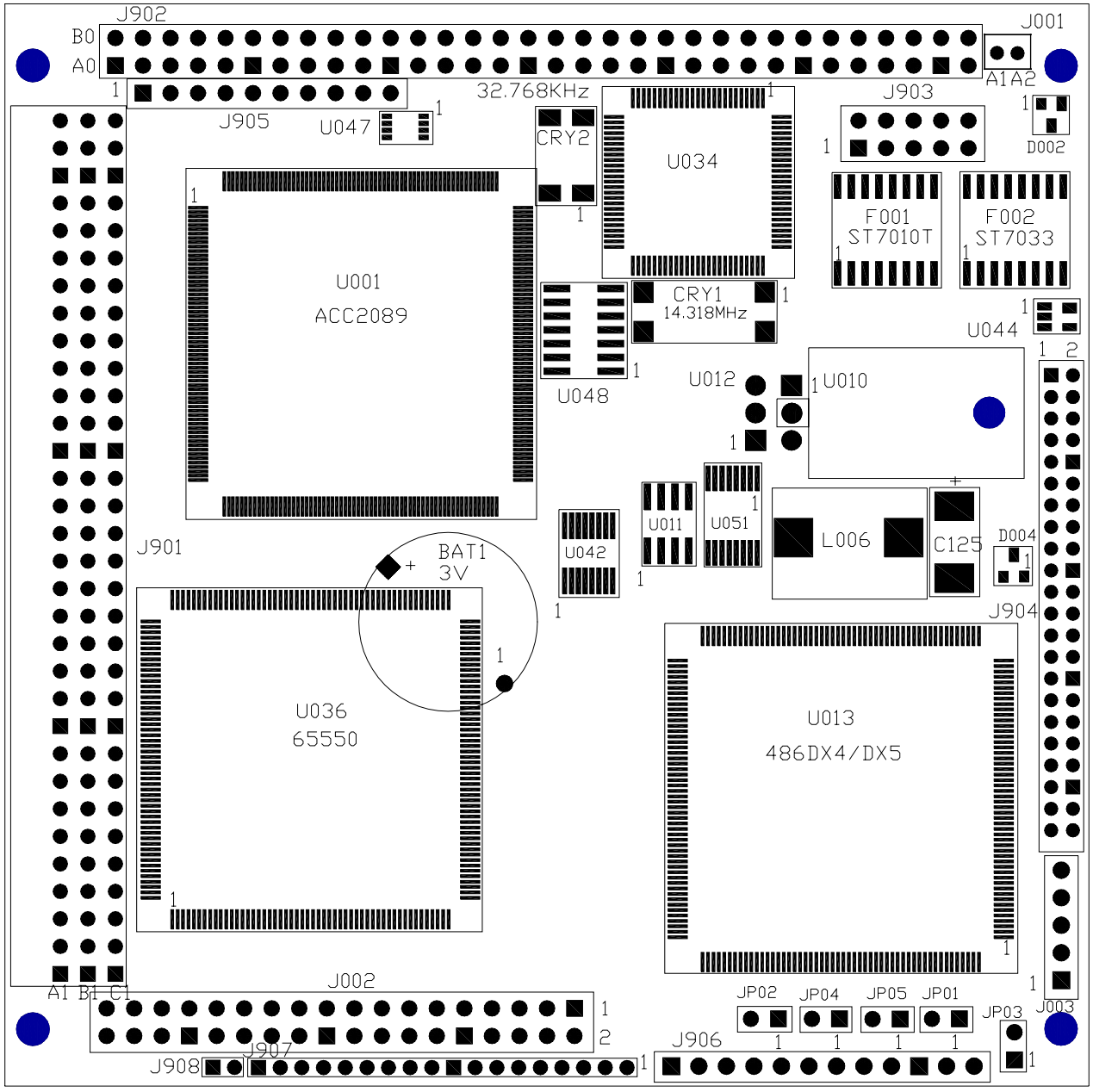


Figure 2 Component Placement – Top Side (v2.10)

6.3 Component Placement – Bottom Side

The following diagram shows the major components on the bottom (solder) side of the PC/II+dxe board.

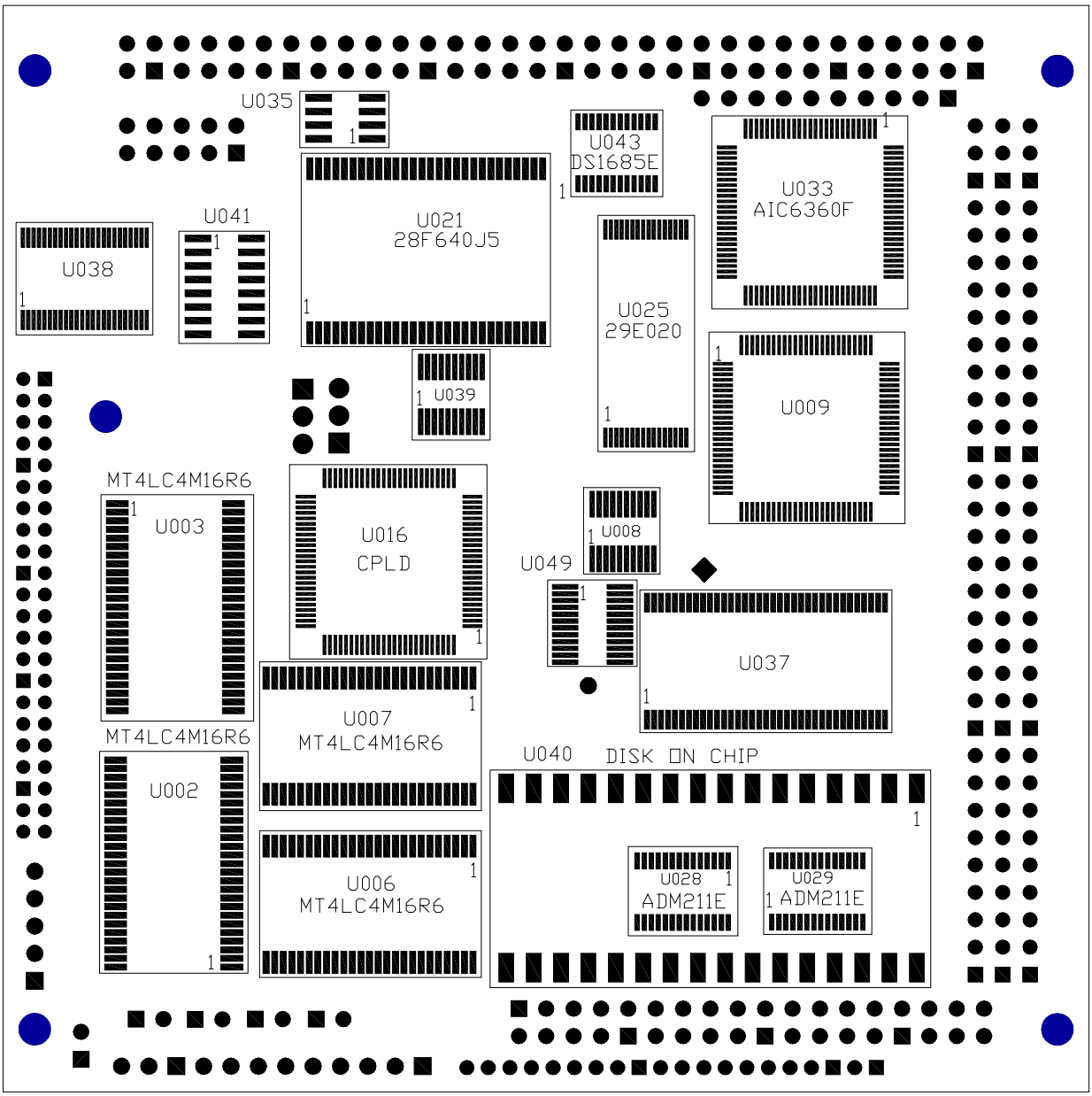


Figure 3 Component Placement – Bottom Side (v2.10)

7 Functional Specification

7.1 Bus, DRAM Memory, Peripheral Controller

PC/II+dxe is shipped with a highly-integrated ACC Micro ACC2089 controller. This controller implements the ISA bus control functionality by bridging the local bus to the ISA 8- and 16-bit bus. It also supports a full memory controller function, and provides standard AT architectural functions. A set of integrated peripheral (super) I/O controllers is also provided.

A description of the various functions of this controller are found in summary form in the corresponding sections of this document. For more detailed specifications, please refer to the ACC2089 datasheet found in the section 2, "Reference Documents" on page 13 of this document.

7.2 Cache Description

Performance is greatly enhanced by the inclusion in the DX4 and DX5 of Enhanced bus mode which provides the capability to support Write-back caching. Either Write-back or Write-Through caching is a selectable manufacturing option (refer to sections 4.2 and 0). All processors implement 16K cache on-chip to provide very fast memory access for both frequent memory accesses to code and/or data. The cache is controlled using a modified MESI protocol, and the cache is implemented as a 'unified' cache to maximize hit ratios when code-to-data ratios are skewed.

7.2.1 Cache Write-through (WT) Mode

Writes and reads to and from system memory are cached. Reads come from cache lines on cache hits; read misses cause cache fills. Speculative reads are allowed. All writes are written to a cache line (when possible) and through to system memory. When writing through to memory, invalid cache lines are never filled, and valid cache lines are either filled or invalidated. This type of cache-control is appropriate for frame buffers or when there are devices on the system bus that access system memory, but do not perform snooping of memory accesses. It enforces coherency between caches in the processors and system memory.

7.2.2 Cache Write-back (WB) Mode

Writes and reads to and from system memory are cached. Reads come from cache lines on cache hits; read misses cause cache fills. Speculative reads are allowed. Write misses cause cache line fills (in the P6 family processors), and writes are performed entirely in the cache, when possible. The write-back memory type reduces bus traffic by eliminating many unnecessary writes to system memory. Writes to a cache line are not immediately forwarded to system memory; instead, they are accumulated in the cache. The modified cache lines are written to system memory later, when a write-back operation is performed. Write-back operations are triggered when cache lines need to be de-allocated, such as when new cache lines are being allocated in a cache that is already full. They also are triggered by the mechanisms used to maintain cache consistency. This type of cache-control provides the best performance, but it requires that all devices that access system memory on the system bus be able to snoop memory accesses to insure system memory and cache coherency.

7.3 Connectors

Connectors can be ordered by specifying one of the standard "Connector System" options (see section 10.1 for ordering information), or they can be custom ordered. The "Connector System" defines standard orientations which will be populated on the board for the basic connectors. Connector Options define the presence and/or detail options for each specific connector.

The following connectors are available by option:

- J001 – Fan (5v) Connector – 1 x 2 (1,25 mm pitch)
- J002 – Panel (Full 24-bit) Connector – 2 x 18 (.100 inch pitch)
- J003 – Alternate +3.3V Power Connector – 1 X 5 (.100 inch pitch)
- J901 – I/O Interface Connector – 3 x 32 (.100 inch pitch)
- J902 – ISA (8-bit) Bus Connector – 2 x 32 (.100 inch pitch)
- J903 – Ethernet Connector – 2 x 5 (.100 inch pitch)
- J904 – IDE Connector – 2 x 22 (2 mm pitch)
- J905 – ISA (16-bit) Bus Extension Connector – 1 x 10 (.100 inch pitch)
- J906 – Alternate +5V Power Connector – 1 x 12 (.100 inch pitch)
- JP05 – Mouse Connector – 1 x 2 (.100 inch pitch)

The "Connector System" options are:

- Option 0 – 96-pin DIN (right-angle) connector, ISA header
- Option 1 – 96-pin & ISA tall headers (for top-mounted QTB)
- Option 2 – 96-pin & ISA sockets (for bottom-mounted QTB)
- Option 3 – 96-pin DIN (right-angle) connector, no ISA connector
- Option 4 – 96-pin header, no ISA connector
- Option 5 – 96-pin stackthrough, ISA sockets, ALL on top
- Option 7 – custom connectors

In the table that follows, we specify a typical connector part number for each type of connector (header, tall header, socket, etc.). While a single source for the type of connector is given in the table, megatel may use a different part from a different supplier. If different parts are shipped by megatel, they will be compatible with the connectors given in the table that follows.

Table 4 Connector Option Part Numbers

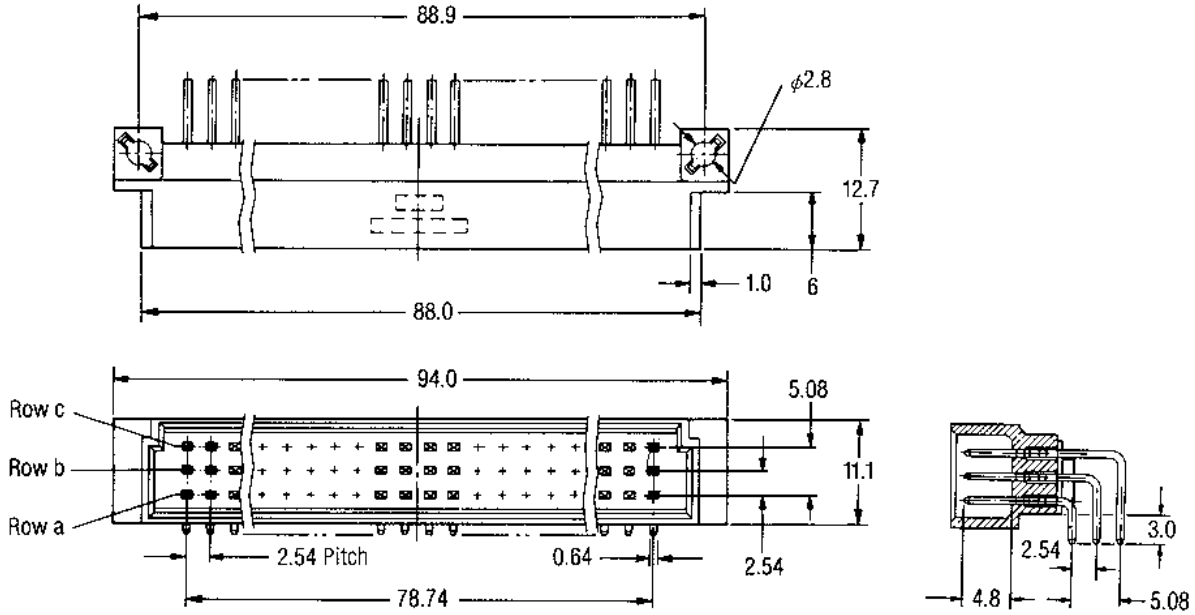
REF[1]	PINS	MOUNT	VENDOR[2]	SAMPLE PART NUMBER[2]	DESCRIPTION
J001	2	CONNECTOR	MOLEX	53057-0210	1x2 1.25 mm RECEPTACLE
J002	36	HEADER	HARWIN	M209981806	2x18 .100 INCH VERTICAL PIN
J003	5	HEADER	HARWIN	M20-9990506	1X5 .100 INCH HEADER
J901	96	DIN R/A	FCI RN	860939671137550E1 DIN-96CPC-SR1-TG30	3x32 .100 INCH DIN R/A MALE
		HEADER– TALL	SAMTEC	EW3209TT300	3X32 .100 INCH VERTICAL PIN
		SOCKET	SAMTEC	SLW13201TD SLW13201TS	2x32 .100 INCH VERTICAL SOCKET 1x32 .100 INCH VERTICAL SOCKET
J902	64	HEADER	HARWIN	M20-9983206	2x32 .100 INCH VERTICAL PIN
		HEADER– TALL	SAMTEC	EW3209TD300	2x32 .100 INCH VERTICAL PIN
		SOCKET	SAMTEC	SLW13201TD	2x32 .100 INCH VERTICAL SOCKET
J903	10	HEADER	HARWIN	M20-998-05-06	2x5 .100 INCH VERTICAL PIN
		HEADER-TALL	HARWIN	M20-998-05-06	2x5 .100 INCH VERTICAL PIN

REF[1]	PINS	MOUNT	VENDOR[2]	SAMPLE PART NUMBER[2]	DESCRIPTION
		SOCKET	SAMTEC	SLW10501TD	2x5 .100 INCH VERTICAL SOCKET
J904	44	HEADER			2x22 2MM VERTICAL PIN
J905	10	HEADER	HARWIN	M20-9991006	1x10 .100 INCH VERTICAL PIN
		HEADER– TALL	SAMTEC	EW1009TS300	1x10 .100 INCH VERTICAL PIN
		SOCKET	SAMTEC	SLW11001TS	1X10 .100 INCH VERTICAL SOCKET
J906	12	HEADER	MOLEX	22-05-2121	1x12 .100 INCH HEADER
JP05	2	HEADER	HARWIN	M20-9990206	1x2 .100 INCH PIN HEADER

NOTES
[1] Nomenclature – REF is part reference number; PINS is part total pin count; MOD is connector model number, which is specified in a field of the board's part number; MOUNT is the generic location of the connector: TOP – on the top side; UP – on the top side to interconnect with a top-mounted accessory board (QTB); DOWN – on the bottom side to interconnect with a bottom-mounted accessory board (QTB).
[2] All connector part numbers are sample values; equivalent connectors may also be used.
[3] Because a wide variety of connectors are available from a large number of sources, Megatel would be pleased to suggest mating connectors or to assist with the selection of custom connectors for your application.

7.3.1 Eurocard DIN 41612– 0.100 Inch Centerline (Right-Angle Plug) Dimensions

The following diagram is representative of a Eurocard DIN 41612 Eurocard 3x32 pin male right-angle connector with 0.100 inch centerline pitch, as provided by AMP. AMP provide a complete line of DIN connectors that can mate to the 96-pin DIN connector used on the PC/II+dxe board.



Shown is the AMP 174111-1 3x32 0.100 inch Type C Eurocard DIN right-angle male connector. Please design to the original drawings for this connector, that are available from AMP and other manufacturers.

7.4 CPLD

PC/II+dxe contains a CPLD device to provide miscellaneous logic that allows the PC/II+dxe to function as an AT-compatible Cpu board.

7.5 Cpu Processor

PC/II+dxe is shipped with a user-selected Intel DX4 or AMD 486DX5 Processor installed. This processor is a full 32-bit pipelined RISC Core, with integrated Floating-Point and Write-Back or Write-Through Cached memory. It provides a high level of performance combined with a low cost base and a rich set of features and Industry Standard 486/386 Compatibility. The 486 family processors support all x86 operating modes, including real mode, native protected mode and virtual mode, and support the full x86 instruction sets, register sets, memory management and I/O management functions. Many frequently-executed instructions take 1 cycle, and pipe-lined architecture allows multiple instructions to execute concurrently. An integrated on-chip floating-point unit supports the full Intel floating-point instruction set and data type set and provides high data rates.

The PC/II+dxe can be shipped with an AMD 486 DX5 that is strapped to operate at 133 MHz processor, or it can be shipped with an Intel 486 DX4 processor strapped to operate at 33 MHz, 50 MHz, 66 MHz or 100 MHz. All standard operating software such as DOS, Windows, Windows 95 or Windows NT4.0 are supported.

DX5 processors and DX4 processors operating at 66 MHz or greater core frequency support host local bus speeds at 33 MHz, providing burst I/O transfers in excess of 100 Million bytes/second. DX4 processors operating at core frequencies of 50 MHz or 33 MHz support host local bus speeds at 16 MHz. Core frequencies are typically 33 MHz, 50 MHz or 66 MHz for lower power applications. The core frequency is a manufacturing option (please refer to "Manufacturing Settings" section 4.2 on page 11).

All peripheral controllers are provided on-board as standard options. Any mix of options can be ordered, which results in a board with the exact price/performance you require.

7.6 DRAM

See section 7.15.

7.7 DRAM Controller

See section 7.1.

7.8 Ethernet Controller

PC/II+dxe contains an optional, highly-integrated LAN Ethernet Interface, that is used in networking applications. This option includes the single-chip Crystal CS8900 controller, a configuration EEPROM, isolation transformers for either 10Base-T and/or AUI, depending upon the option ordered, and an on-board Ethernet header (J903).

PC/II+dxe pulls the Attachment Unit Interface (AUI) port signals and the 10Base-T twisted-pair port signals to a 10-Pin (2x5 on 0.100" [2,54 mm] spacing) on-board header. When connected to the megatel Ethernet Paddle Board (an accessory board product), the AUI port signals are pulled to a DB15 connector and the 10Base-T port signals are pulled to an RJ-45 connector. Please refer to the section 9.6, "
J903 – Ethernet Connector", on page 90 of this document for a description of the Ethernet header pins.

The AUI port can be connected to an Ethernet Transceiver cable drop to provide a fully IEEE 802.3 AUI interface, while the 10Base-T interface also fully complies to IEEE 802.3.

The CS8900 controller contains an IEEE 802.3 MAC engine that operates in the I/O address space. It contains an on-chip RAM for buffering receive & transmit frames, and supports full duplex operation, a 10BASE-T port with analog filters & automatic polarity correction, and an AUI port. Programmable transmit features include automatic re-transmission on collision, and automatic padding and CRC generation. Programmable receive features include Automatic-switch between DMA & on-chip memory, early interrupts for frame preprocessing, and automatic rejection of erroneous packets. An on-board configuration EEPROM is provided for jumper-less configuration, and on-board transformers for each interface are provided. The CS8900 supports I/O transfers at up to 10 Megabits/sec. Depending upon which media is active, the AUI or 10Base-T interface is automatically enabled. This automatic selection can be overridden by software configuration.

Drivers for most operating systems, including DOS, Windows and NT, are available.

For detailed specifications of the Ethernet Controller and Interface, please refer to the datasheets for the Ethernet Controller and Isolation Transformers, found in section 2, "Reference Documents" on page 13 of this document. Refer also to the Megatel "Ethernet Appbook", document number MT004702.

7.9 Flash ROM – BIOS

The standard ROM on the PC/II+dxe is a 2Mbit (256K Byte) flash EEPROM. A 128K Byte flash EEPROM for BIOS may also be shipped for some models. The BIOS EEPROM contains the system BIOS and all option BIOS modules, including the SVGA BIOS, the SCSI BIOS and other bios modules required to interface to on-board peripherals. All PC/II+dxe boards are shipped with a flash BIOS.

BIOS code is shadowed in system memory located between C0000h and FFFFFh. The system BIOS code occupies the top segment of real mode memory (F0000h to FFFFFh). Option ROM BIOS modules are shadowed into the region C0000h to DFFFFh. Option BIOS modules will be loaded depending upon the configuration of the PC/II+dxe board.

The following tables describe the drivers that are available for use with the PC/II+dxe board. Both drivers and optional ROM BIOS modules are listed. Please contact Megatel if you have specific requirements, and to receive the driver information, or visit our Website.

Table 5 ETHERNET Drivers & Utilities

DRIVER NAME	REVISION
Netware ODI DOS Client	2.62
Netware ODI OS/2 Client	2.59
Netware ODI Server Driver	2.60
OS/2 NDIS2 Driver	2.68
DOS NDIS2 Driver	2.68
Windows NT/95 NDIS3 Driver	3.20
Windows for Workgroup NDIS3 Driver	2.57
Packet Driver	2.55
Setup utility	2.66

Table 6 VIDEO Drivers & BIOS Options

DRIVER NAME	REVISION
HiQVideo Driver for Win NT 3.5x	1.1.5
HiQVideo Driver for Win 95	1.2.6
Display Driver for Windows 3.x	1.3.2
Display Driver for OS/2	2.2.7

DRIVER NAME	REVISION
HiQVideo VGA BIOS	2.0.0

Table 7 FLASH Array BIOS Option

DRIVER NAME	REVISION
Datalight CardTrick (as Optional ROM)	3.01.13

7.10 Flash ROM – User

PC/II+dxe contains an optional 2MB, 4MB or 8MB of Flash Array. PC/II+dxe uses Intel® StrataFlash™ or FlashFile™ high-density symmetrically-blocked architecture flash memory. Flash Array parts are soldered on the circuit board. The flash array is supported by the Datalight Cardtrick BIOS driver.

All required programming voltages are provided on-board.

7.11 Flash Disk – M-Systems Disk-on-Chip

PC/II+dxe contains an optional 32-Pin DIP socket that can be user-populated with a M-Systems Disk-on-Chip® 2000 flash disk. The socket is bottom-mounted on the PC/II+dxe circuit board.

The Disk-on-Chip® product provides standalone or expansion Flash Disk memory in sizes ranging from 2 to 144 MB.

Both the DiskOnChip® 2000 and Flash Array can be used together on the same board.

For more detailed information on Disk-on-Chip® products, please contact M-Systems.

7.12 Floppy Disk Interface

PC/II+dxe contains a Floppy Disk Drive Interface controller as part of the basic board, provided by the ACC Micro ACC2089. Floppy disk interface signals are pulled to the Peripheral I/O Connector.

The controller supports one (1) or two (2) 3.5" floppy disk drives. It is compatible with IBM System 34 double density format (MFM), and Sony EMCA format. Address decoding is compatible with the IBM PC drive system. Both DMA and non-DMA modes are supported. Standard 500, 250 and 300 Kb/Sec transfer rates are supported.

The Floppy Disk controller uses Interrupt Request IRQ6, and DMA channel DRQ2.

The floppy disk interface can be multiplexed to the parallel port pins for external floppy disk drive support. This function is enabled by setting Register BEh, Bit 2, to one.

For more detailed information about the Floppy Disk Interface, please refer to the ACC2089 datasheet, found in section 2, "Reference Documents" on page 13 of this document.

7.13 ISA Bus Interface

The PC/II+dxe optionally supports the 8-bit ISA (XT/AT) bus and a 16-bit extension for I/O access to peripheral cards. The ISA bus is pulled to J902 (8-bit bus) and J905 (16-bit extension). The ISA bus can be software-configured to operate at one of the following clock speeds:

Table 8 Pinout – ISA 8-bit Bus J902 (Rows A and B) – 2 X 32 .100" Header

ISA BUS CLOCK SPEED	CONFIGURATION VALUE [1]
3.33 MHz	10000
4.16 MHz	10101
5.53 MHz	10001
6.66 MHz	10010
7.71 MHz	0XXXX
8.00 MHz (default speed set by BIOS)	11XXX
8.32 MHz	10111
11.11 MHz	10011
16.66 MHz	10100
16.66 MHz	10110

NOTES

[1] *Binary format. This value is written to the 2089 register 0x05 (bits 4:0). 'X' = don't care value.*

A description of this bus implementation, and differences from the old XT/AT bus, is provided in the Connectors section of this document. Please refer to section 9.5 on page 82 for the 8-bit ISA bus connector, and to section 9.8 on page 95 for the 16-bit ISA bus extension connector.

7.14 LEDs

PC/II+dxe contains up to three (3) LEDs:

- **D2** contains two separate LEDs to indicate the status of the Ethernet Line Activity and Ethernet Local Activity – refer to section 7.5 on page 35 for more information.
- **D4** is a System LED that indicates (when lit) the status of the hardware. The Bios controls this LED.

7.15 Memory

The PC/II+dxe board is shipped with a user-specified amount of EDO 60 ns DRAM parts. There are 4 population sites on the board for the two banks of soldered-down EDO DRAM. Either 1Mx16 or 4Mx16 parts are installed. The memory controller within the ACC2089 operates on the local bus at 33 MHz.

The amount of soldered and socketed memory on a given board is automatically detected by the BIOS.

The valid combinations of populated & socketed memory by total memory given in the following table.

Table 9 Total System Memory Options

TOTAL	DEVICES x ORGANIZATION
4 MB	2 x 1Mx16 EDO 60ns
8 MB	4 x 1Mx16 EDO 60ns
16 MB	2 x 4Mx16 EDO 60ns
32 MB	4 x 4Mx16 EDO 60ns

NOTES
[1] Boards may be shipped with alternately-sourced parts and specifications may differ; for example, 50ns EDO parts may be shipped on some boards depending upon current availability and pricing of parts.

7.16 Parallel Port

PC/II+dxe supports a single Parallel Port controller that is integrated in the ACC2089 super I/O. The parallel port is a basic feature of PC/II+dxe. It is pulled to the 96-pin DIN I/O Connector.

The parallel port interface supports a standard selectable ECP/EPP/BPP/SPP mode. It is software configurable – there are no jumpers required. The parallel port supports standard Centronics-type printers, standard PS/2-type Bi-directional devices, and Enhanced Parallel Port (EPP 1.9) and Extended Capabilities Port (ECP) protocols.

A 16-byte FIFO is included in the interface, used by EPP and ECP modes. Run-Length Compression (RLE) is also supported. Both DMA and PIO transfers are supported.

For detailed specifications on the operation of the Parallel Port, please refer to the datasheets for the ACC2089, found in section 2, "Reference Documents" on page 13 in this document.

7.17 Peripheral Controller

See section 7.1.

7.18 Power Monitor

See section 7.27.

7.19 Processor

See section 7.5.

7.20 Real-Time Clock

The PC/II+dxe contains an optional Real-Time Clock (RTC), a Dallas Semiconductor DS1685. This clock is a full-function part, and is certified as Year-2000 compliant by Dallas. The RTC uses a 32.768 KHz crystal and a 3.0V Lithium battery. The battery is soldered onto the circuit board and is part of the RTC option.

Information contained in the following sub-sections is present in summary form. For more detailed information about the Real-Time Clock, please refer to the DS1685 datasheet found in section 2, "Reference Documents" on page 13 of this document.

7.20.1 Features of the Real-Time Clock

- 242 Bytes battery backed up NVRAM
- RAM Clear input
- Low battery current (500 nA)
- Leap Year to year 2100 provides Year 2000 compliance
- Century byte with Automatic Rollover provides Year 2000 compliance
- 24 0r 12 Hour Format
- Programmable Alarm, Settable at Any Time hh:mm:ss, with Interrupt
- Programmable Timer, Settable to Periods Ranging from 122 uSec to 500 mSec
- Daylight Savings Time Support
- Unique 48-Bit Silicon Laser-Written Serial Number, Can be used by Customer Applications

The PC/II+dxe is factory-shipped with the Real-Time Clock set to the correct time and date for the North-American EST (Eastern Standard Time) time zone. The software for the Real-Time Clock is included in the system BIOS for boards containing the Real-Time Clock option.

The Lithium battery is rated for 125 mAh (typical) in an operating range of -20C to +70C. Discharge current is 500 nA, and storage temperature is -40C to +60C.

7.20.2 Setting Time and Date

The DOS clock is updated automatically by the Real-Time Clock upon Boot-Up. Should you change the time or date in DOS, the PC/II+dxe will conversely update the Real-Time Clock hardware time and date. The PC/II+dxe uses standard DOS instructions to change the time and date. If you are using standard DOS, and if the time and date are displayed at boot time, you may at that point change the time and date if desired. Standard DOS commands to change the TIME and DATE can also be used.

Time and date are also settable in Windows and Windows NT4.0; please refer to the operating system documentation for details.

7.20.3 Using the Real-Time Clock NVRAM

The BIOS utilizes the battery backed up NVRAM to store its configuration information which it needs to access at boot time and at other times. Besides the time and data information contained in the Real-Time Clock hardware, the BIOS stores information about the Video preferences, floppy disk drive configuration, and panel information.

A total of 114 Bytes of RAM in bank 0, and 128 Bytes of RAM in bank 1 are supported (total of 242 Bytes of RAM).

7.20.4 Real-Time Clock Interrupt 1Ah

The BIOS supports AT compatible real-time clock functions using software interrupt 1Ah. In addition, the PC/II+dxe BIOS supports the following functions using the software interrupt 1Ah, which provide read and write access to bank 0 and bank 1 SRAM memory in the real-time clock, and read access to the unique serial number encoded in the real-time clock chip.

1. FUNCTION 0FFh – WRITE AND READ BANK-0 SRAM

This function writes a byte to RTC SRAM Bank 0, or reads a byte from RTC SRAM Bank 0.

```
MOV     AH,0FFh
MOV     DL,<RTC bank 0 register number>
MOV     DH,<Direction>                  Bit 0 = 0 (WRITE), Bit 0 = 1 (READ)
                                        Bit 1-7 = Unused
MOV     AL,<8-Bit Value to be Written>  Used if DH.0 = 0, Unused if DH.0 = 1
INT     1Ah
-- returns here with
        /FX.CF = 1 (Error)
        /FX.CF = 0 (No Error)
                /AH = Destroyed
                /AL = value read from RTC or written to RTC>
```

2. FUNCTION 0FBh – WRITE AND READ BANK-1 EXTENDED SRAM

This function writes a byte to RTC Bank 1 Extended SRAM, or reads a byte from RTC Bank 1 Extended SRAM.

```
MOV     AH,0FBh
MOV     DL,<RTC bank 1 register number>  0 - 7Fh
MOV     DH,<Direction>                  Bit 0 = 0 (WRITE), Bit 0 = 1 (READ)
                                        Bit 1-7 = Unused
MOV     AL,<8-Bit Value to be Written>  Used if DH.0 = 0, Unused if DH.0 = 1
INT     1Ah
-- returns here with
        /FX.CF = 1 (Error)
        /FX.CF = 0 (No Error)
                /AH = Destroyed
                /AL = value read from RTC or written to RTC>
```

3. FUNCTION 0FCh – READ RTC SERIAL NUMBER

This functions reads the silicon serial number that is embedded in the RTC chip. Each RTC chip is manufactured to contain a unique serial number.

```
MOV     AH,0FCh
LES     DI,<pointer to seven-byte buffer that will receive the serial number field>
INT     1Ah
-- returns here with
        /FX.CF = 1 (Error)
        /FX.CF = 0 (No Error)
                /[ES:DI+0] = Silicon Serial Number Byte 1 through Byte 6
                /[ES;DI+6] = Silicon Serial Number CRC byte
```

7.20.5 Real-Time Clock Memory Map

Table 10 Real-Time Clock Memory Map

RTC Offset	Bank 0		Bank 1	
	Description	Access	Description	Access
00	Seconds	R(bits 0-7), W(bits 0-6)	Seconds	R(bits 0-7), W(bits 0-6)
01	Seconds Alarm	RW	Seconds Alarm	RW
02	Minutes	RW	Minutes	RW
03	Minutes Alarm	RW	Minutes Alarm	RW
04	Hours	RW	Hours	RW
05	Hours Alarm	RW	Hours Alarm	RW
06	Day of the Week	RW	Day of the Week	RW
07	Day of the Month	RW	Day of the Month	RW
08	Month	RW	Month	RW
09	Year	RW	Year	RW
0A	Register A	R(bits 0-7), W(bits 0-6)	Register A	R(bits 0-7), W(bits 0-6)
0B	Register B	RW	Register B	RW
0C	Register C	R	Register C	R
0D	Register D	R	Register D	R
0E-3F	RAM Bytes 00-3F		RAM Bytes 00-3F	
40	RAM Byte 40		RTC Model Number	
41	RAM Byte 41		1st Byte Serial Number	
42	RAM Byte 42		2nd Byte Serial Number	
43	RAM Byte 43		3rd Byte Serial Number	
44	RAM Byte 44		4th Byte Serial Number	
45	RAM Byte 45		5th Byte Serial Number	
46	RAM Byte 46		6th Byte Serial Number	
47	RAM Byte 47		CRC Byte	
48	RAM Byte 48		Century Byte	
49	RAM Byte 49		Date Alarm	
4A	RAM Byte 4A		Extended Control Reg 4A	
4B	RAM Byte 4B		Extended Control Reg 4B	
4C	RAM Byte 4C		Reserved	
4D	RAM Byte 4D		Reserved	
4E	RAM Byte 4E		RTC Address - 2	

RTC Offset	Bank 0		Bank 1	
	Description	Access	Description	Access
4F	RAM Byte 4F		RTC Address - 3	
50	RAM Byte 50		Extended RAM Address	
51	RAM Byte 51		Reserved	
52	RAM Byte 52		Reserved	
53	RAM Byte 53		Extended RAM Data Port	
54-7F	RAM Bytes 54-7F		Reserved	

Table 11 RTC Extended RAM Memory Map

Via 50 & 53	Bank 0		Bank 1 Extended RAM	
00-7F	-		RAM Bytes 00-7F	RW

7.21 SCSI Controller

PC/II+dxe contains an optional SCSI-2 controller. The SCSI-2 bus signals are pulled to the 96-pin DIN I/O Connector.

The SCSI-2 controller is used as the Host device on a SCSI-2 bus. This controller supports byte, word or 32-bit double word PIO data transfers, and can also utilize 16-bit DMA. With its 128-byte data FIFO, it can burst data at up to 10 MBytes/s across the Host bus, and can support synchronous data transfers at up to 10 MBytes/s across the SCSI bus.

The SCSI interface uses Interrupt Request IRQ11, and DMA channel DRQ6.

Please contact megatel for information on this feature.

7.22 Serial Ports

PC/II+dxe contains 1 or 2 optional full RS-232E ports, and an optional BIOS-accessible 2-wire RS-232 port. The serial port options include RS-232 receivers and line drivers for the respective ports which are ordered.

7.22.1 COM1 & COM2

Serial COM1 and COM2 ports are fully 16C550 compatible, and contain standard modem control and data I/O interface signals.

PC/II+dxe uses the ADM211E receiver/driver on COM1 and COM2 serial interfaces to provide RS-232 levels. The transceiver is EIA-RS232E and CCITT V.28 compliant. Input tolerance on all inputs is ±25V, and output swing on all outputs is ±9V with all transmitter outputs loaded with 3K ohms to Ground. The transceivers run at +5V and use on-chip voltage doublers and inverters. Refer to the ADM211E datasheet for determining the power which may be drawn by attached devices.

Each port contains both receive and transmit FIFOs which are 16-bytes deep.

These two I/O ports are configured by the BIOS as COM1 and COM2.

COM1 uses Interrupt Request IRQ4, and is based in I/O address space at 3F8h. COM2 uses Interrupt Request IRQ3, and is based in I/O address space at 2F8h.

For more detailed information about serial I/O, please refer to the ACC2089 datasheet, found in section 2, "Reference Documents" on page 13 of this document.

7.22.2 COM4

A special 2-wire serial I/O port is provided by the hardware and is supported by the PC/II+dxe BIOS (INT 14h). This port contains RXD and TXD (Receive Data and Transmit Data serial data signals) which are pulled out to the 96-pin DIN Peripheral I/O connector. Modem control signals not used on this 2-wire interface and modem status bits returned by INT 14h functions show the port as always on and ready to transmit data.

The line driver and receiver for this port supports true RS-232 to/from CMOS voltage conversion. The driver and receiver are supported by an ADM211E; refer to the datasheet for this device for more information, found in section 2, "Reference Documents" on page 13 of this document.

This I/O port is configured by the BIOS as COM4.

COM4 uses either non-interrupt I/O (also referred to as Polling) or Hardware Interrupt Request IRQ9. Normally, the BIOS interrupt 0x14 uses Polled I/O, and ANY call to function 0 of software interrupt 0x14 will cause both the transmit and receive interrupts to be disabled (masked). If you wish to enable interrupt processing (using IRQ9) for the two-wire COM4 serial port, you should perform the following I/O sequence (shown in assembler code) or equivalent:

```
MOV    DX,098Ch
IN     AL,DX
<set or reset the Transmitter and/or receiver interrupt mask bits>
OUT    DX,AL
```

where port 0x98C is defined as follows:

BITS 7-2:	Reserved, do not change
BIT 1:	COM4 Transmit Interrupt Mask (0=Unmask/Enable, 1 = Mask/Disable)
BIT 0:	COM4 Receive Interrupt Mask (0=Unmask/Enable, 1 = Mask/Disable)

The two-wire COM4 Serial I/O port on the PC/II+dxe generates an interrupt under these conditions: (a) the Receiver is Enabled, the Receive Buffer is Full, and Receive Interrupts are Unmasked, and (b) the Transmitter is Enabled, the Transmit Buffer is Empty, and Transmit Interrupts are Unmasked.

7.23 Speaker Output

Output sound waveform signals carried by the Speaker Output signal are generated by Timer 2. The Timer 2 output is gated with port 0x60, bit 1 (Speaker Data) to drive the Speaker Output. The state of Timer 2 output can be read from port 0x61, bit 5.

Speaker Output signal is pulled to the 96-pin DIN I/O Connector (PC-SPKROUT, J901, pin A9). It is intended to drive a piezo-electric audio transducer connected between the Speaker Output signal pin and Ground.

7.24 Super AT I/O Controller

AT Super-I/O functionality is provided by the ACC MICRO 2089 and is part of the basic board functionality. This controller provides 2 full 16550-style UARTs with 16-byte FIFOs (full on-board RS232 transceivers are supported), a Parallel ECP/EPP port (also configurable as BPP/SPP), a PS/2-style Keyboard and PS/2 Mouse, an IDE controller with support for two devices, and a standard Floppy controller with support for two 3.5” drives. Additional standard features include generation of PC speaker output, and system reset switch input.

The functionality provided by the Super I/O controller is described in their respective sections in this document.

7.25 Timers/Counters

Three internal counters are provided as basic features of PC/II+dxe. The timers/counters are compatible to the AT standard 8254. The clock input for each is tied to a clock of 1.193 MHz, which is derived by dividing the system 14.31818 MHz clock by 12, and which provides a minimum timing resolution of 838 ns.

Timer 0 output is tied to IRQ0 (Interrupt controller 1, level 0).
Timer 1 output is used to initiate a refresh cycle for system memory.
Timer 2 is used to generate signals that produce sound waveforms on the Speaker Output signal.

7.26 Video – CT 65550 Super VGA & Panel Controller

The PC/II+dxe board can be shipped with the Video option to provide the compatible video interface using the megatel 96-pin DIN connector, J901. The board can also be shipped with a new video interface connector for the 4x4Family, J002, that fully supports 8-bit through 24-bit panels. The board can also be shipped with either a 5V or a 3.3V panel interface.

The **compatible video interface** is provided on the 96-pin DIN connector, J901, and consists of either a pre-configured 8-bit or 16-bit (multiplexed) panel interface, or an Analog (CRT) video interface. Pre-configuration of this interface for panel support is specified when the board is ordered from the factory. The analog interface is multiplexed on the 96-pin DIN connector with the 8/16-bit 65530-style panel signals, using the ENAVEE control signal (which is a programmable signal) to control when it is active: when ENAVEE is active (for the Chips® 65550 Video Controller, ENAVEE is active high), the Panel signals are presented on the connector; when ENAVEE is inactive, the Analog signals are presented on the connector.

Note that the ENAVEE signal is also made available on the 96 pin DIN connector pin A3 and A5 using options "j" and "k" respectively, and also on the LCD 24-bit panel connector, J002, pin 31. The polarity of the signal that is output to these three pins can be selected by option "n". If using the "compatible video" interface on the 96-pin DIN connector, ENAVEE should be set to active low.

The **24-bit panel interface** is provided using an on-board 2x18 .100 inch header, J002. This interface supports all panel types and panel modes supported by the C&T 65550 video controller. This interface may be used regardless of the configuration or mode of the compatibility video interface.

The Video Interface option includes 2MB of fast video memory EDO DRAM.

The Video panel interface can be ordered to support either 5V panels or 3.3V panels. This option affects both the 24-bit panel interface and the compatible video interface. For more information on using the 3.3V panel interface, contact Megatel Engineering.

7.26.1 Video Hardware Overview

The PC/II+dxe Video Interface uses the Chips® 65550 Video Controller and is compatible with the IBM-PS/2 Video Graphics Array (VGA) and supports the SVGA standard. The controller operates on the local bus, and supports both Analog Monitors and a wide variety of Flat Panels. It contains a powerful 64-bit Graphics Engine, Palette/DAC and Clock Synthesizer. The separate 2MB of fast EDO DRAM video memory is accessed from the controller over a direct 32-Bit bus. This video memory is used normally, to buffer all video data and is mapped by the controller into Main memory address space. It is also used for frame buffering in LCD-DD interfaces – unused video memory is automatically used for a framestore area by the controller in this case. The hardware register and gate interface is standard VGA, and the BIOS is also VGA compatible. Drivers for all common operating systems are available. Simultaneous CRT and LCD display mode is available.

7.26.2 Video Hardware Features

Please refer to the Chips® 65550 reference documentation for a list of features available. The 65550 supports these features (revision 1.5, December 1997):

- Highly integrated design Flat Panel and CRT GUI Accelerator & Multimedia Engine, Palette/DAC, and Clock Synthesizer
- Hardware Windows Acceleration
    - 64-bit Graphics Engine
      – System-to-Screen and Screen-to-Screen BitBLT
      – 3-Operand Raster-Ops
      – 8/16/24 Color Expansion

    - Transparent BLT
      – Optimized for Windows™ BitBLT format
- High Performance:
    - Deep write buffers
    - EDO DRAM Support
    – 40 MHz
- Display centering and stretching features for optimal fit of VGA graphics and text on 800x600 and 1024x768 panels
- Simultaneous Hardware Cursor and Pop-up Window
    - 64x64 pixels by 4 colors
    - 128x128 pixels by 2 colors
- Game Acceleration
    - Source Transparent BLT
    - Destination Transparent BLT
    - Double buffer support for YUV and 15/16bpp Overlay Engine
    - Instant Full Screen Page Flip
    - Read back of CRT Scan line counters.
- Optimized for High-Performance Flat Panel Display at 3.3V
    - 640x480 x 24bpp
    - 800x600 x 24bpp
    - 1024x768 x 16bpp
- CRT Support to 80 MHz at 3.3V
- Direct interface to Color and Monochrome, Single Drive (SS), and Dual Drive (DD), STN & TFT panels
- Flexible On-chip Activity Timer facilitates ordered shut-down of the display system
- Composite NTSC / PAL Support
- Power Sequencing control outputs regulate application of Bias voltage
- Fully Compatible with IBM® VGA

7.26.3 Video Driver Features

- High Performance Accelerated drivers
- Compatible across HiQVideo family
- Auto Panning Support
- LCD/CRT/Simultaneous Mode Support
- Auto Resolution Change
- HW Stretching/Scaling
- Double Buffering
- Internationalization
- ChipsCPL (Control Panel Applet)
- Direct Draw support
- Games SDK support
- Dynamic Resolution Switching
- VGA Graphics applications in Window
- VESA DDC extensions
- VESA DPMS extensions
- Property Sheet to change Refresh/Display
- Seamless Windows Support
- Boot time resolution adjustment
- DIVE, EnDIVE
- DCAF
- DebugVGA
- Auto testing of all video modes
- ChipsVGA

- ChipsEXT
- BIOS OEM Reference Guide
- Display Driver User's Guide
- Utilities User's Guide
- Release Notes for BIOS, Drivers, and Utilities

7.26.4 Video BIOS Features

- VGA Compatible BIOS
- DDC 1, DDC 2AB
- Text and Graphics Expansion
- Auto Centering
- 44 (40) K BIOS
- CRT, LCD, Simultaneous display modes
- Auto Resolution Switch
- Multiple Refresh Rates
- NTSC/PAL support
- Extended Modes
- Extended BIOS Functions
- 1024x768 TFT, DSTN Color Panels
- Multiple Panel Support (8 panels built in)
- Get Panel Type Function
- HW Popup Interface
- Monitor Detect
- Pop Up Support
- SMI and Hot Key support
- Set Active Display Type Hook
- Save/Restore Video State Hook
- Setup Memory for Save/Restore Hook
- SMI Entry Point Hook
- Int 15 Calls after POST, Set Mode Hook

7.26.5 Video Display Enhancement Features

A variety of video enhancement features are supported, particularly for flat panels, by the Chips® 65550 Video Controller:

True-Gray

PC/II+dxe video supports TRUE-GRAY gray scale algorithm, a polynomial-based frame-rate control (FRC) and dithering algorithm to generate a maximum of 61 gray levels on monochrome panels. This algorithm extends the support of flicker-free gray scales from 16 to 61 on, for example, film-compensated monochrome STN LCDs, without the need to increase refresh rate, a conventional solution which increases power consumption, ghosting and decreases contrast.

RGB Color to Gray Scale Reduction

PC/II+dxe video supports RGB Color to Gray Scale Reduction, allowing 24-bit color pallette data to be reduced automatically to 6-bits for 64 gray scales. Reduction techniques include NTSC weighting, Equal Weighting (for blue background operating systems such as Windows), and Green Only for replicating 6-bits of green pallette data such as IBM monochrome monitors.

SmartMap

PC/II+dxe video supports SMARTMAP, an algorithm that automatically adjusts the foreground and background of adjacent gray scales to maximize contrast on flat panel displays. This algorithm is particularly useful when displaying information containing multiple colors on monochrome flat panels.

Text Enhancement

PC/II+dxe video supports Text Enhancement whereby Dim White is displayed on flat panels as Bright White to optimize contrast level.

Vertical Compensation

PC/II+dxe video supports Vertical Compensation techniques for flat panels. Unlike CRT monitors, flat panels have a fixed number of scan lines (eg. 200, 400, 480 or 768 lines). PC/II+dxe allows lower resolution software to be displayed on a higher resolution panel by use of manual or automatic Vertical Centering, Stretching, Blank Line Insertion, or Tall Font™.

Horizontal Compensation

PC/II+dxe video supports Horizontal Compensation techniques for flat panels, including Horizontal Compression, Horizontal Centering and Horizontal Doubling and text expansion.

7.26.6 Video Analog CRT Display Support

The Analog CRT interface is provided on the 96-pin DIN connector, J901, and may be used when the compatible panel interface on the 96-pin DIN connector is not being used (use of the Analog CRT video interface may occur simultaneously with a panel attached to J002, the 8/16/24-bit panel interface).

PC/II+dxe supports high resolution fixed frequency and variable frequency analog monitors in interlaced and non-interlaced modes of operation. The video controller supports up to 80 MHz at 3.3V, which provides SVGA resolutions up to 1280 x 1024 – 256 colors, 1024 x 768 – 256K colors or 800 x 600 – 1,677,216 colors. Please refer to the Chips® 65550 documentation for detailed information.

All standard VGA modes are supported on these typical CRT monitors: PS/2 fixed frequency analog CRT monitor or equivalent (31.5 / 33.5 KHz horizontal frequency specification); NEC Multi-Sync 3D or equivalent multi-frequency CRT monitor (37.5 KHz minimum horizontal frequency specification); Nanao Flexscan 9070s, Multisync 5D, or equivalent multi-frequency high-performance CRT monitor (48.5 KHz minimum horizontal frequency specification).

7.26.7 Video Flat Panel Display Support – 8/16/24-bit 2x18 Panel Connector

This section applies to panels attached to the 8/16/24-bit panel connector, J002.

The on-board Chips 65550 controller supports all flat panel display technologies, including plasma, electroluminescent (EL) and liquid crystal (LCD). LCD panel interfaces are provided for single panel, single drive (SS) and dual panel, dual drive (DD) configurations.

The controller utilizes the on-board video memory for its integrated frame buffer and 24-bit panel interface; the "C" DRAM is not used on the PC/II+dxe.

Standard and high-res passive STN and active matrix TFT/MIN LCDs are supported. Up to 16M colors on 24-bit active matrix LCDs, up to 4K colors on passive STN LCDs and up to 64 gray scales on monochrome panels are supported.

The flat panel interface can interface to a variety of panels, as illustrated in the following table; please refer to the Chips® 65550 Video Controller reference documentation for details.

Table 12 Flat Panel Interface Signal Mapping

J002 Pin#	J002 Pin Name	Mono SS 8-bit	Mono DD 8-bit	Mono DD 16-bit	Color TFT 9/12/ 16 bit	Color TFT 18/24 bit	Color TFT HR 18/24 bit	Color STN SS 8-bit (x4bP)	Color STN SS 16-bit (4bP)	Color STN DD 8-bit (4bP)	Color STN DD 16-bit (4bP)	Color STN DD 24-bit	65550 Pin#	65550 Pin Name
26	L1-FPD0	–	UD3	UD7	B0	B0	B00	R1 - G1	R1	UR1	UR0	UR0	71	P0
25	L1-FPD1	–	UD2	UD6	B1	B1	B01	B1 - R2	G1	UG1	UG0	UG0	72	P1
24	L1-FPD2	–	UD1	UD5	B2	B2	B02	G2 - B2	B1	UB1	UB0	UB0	73	P2
23	L1-FPD3	–	UD0	UD4	B3	B3	B03	R3 - G3	R2	UR2	UR1	LR0	74	P3
22	L1-FPD4	–	LD3	UD3	B4	B4	B10	B3 - R4	G2	LR1	LR0	LG0	75	P4
21	L1-FPD5	–	LD2	UD2	G0	B5	B11	G4 - B4	B2	LG1	LG0	LB0	76	P5
20	L1-FPD6	–	LD1	UD1	G1	B6	B12	R5 - G5	R3	LB1	LB0	UR1	78	P6
19	L1-FPD7	–	LD0	UD0	G2	B7	B13	B5 - R6	G3	LR2	LR1	UG1	79	P7
18	L1-FPD8	P0	–	LD7	G3	G0	G00	SHFCLKU	B3	–	UG1	UB1	81	P8
17	L1-FPD9	P1	–	LD6	G4	G1	G01	–	R4	–	UB1	LR1	82	P9
16	L1-FPD10	P2	–	LD5	G5	G2	G02	–	G4	–	UR2	LG1	83	P10
15	L1-FPD11	P3	–	LD4	R0	G3	G03	–	B4	–	UG2	LB1	84	P11
14	L1-FPD12	P4	–	LD3	R1	G4	G10	–	R5	–	LG1	UR2	85	P12
13	L1-FPD13	P5	–	LD2	R2	G5	G11	–	G5	–	LB1	UG2	86	P13
12	L1-FPD14	P6	–	LD1	R3	G6	G12	–	B5	–	LR2	UB2	87	P14
11	L1-FPD15	P7	–	LD0	R4	G7	G13	–	R6	–	LG2	LR2	88	P15
10	L1-FPD16	–	–	–	–	R0	R00	–	–	–	–	LG2	90	P16
9	L1-FPD17	–	–	–	–	R1	R01	–	–	–	–	LB2	91	P17
8	L1-FPD18	–	–	–	–	R2	R02	–	–	–	–	UR3	92	P18
7	L1-FPD19	–	–	–	–	R3	R03	–	–	–	–	UG3	93	P19
6	L1-FPD20	–	–	–	–	R4	R10	–	–	–	–	UB3	94	P20
5	L1-FPD21	–	–	–	–	R5	R11	–	–	–	–	LR3	95	P21
4	L1-FPD22	–	–	–	–	R6	R12	–	–	–	–	LG3	96	P22
3	L1-FPD23	–	–	–	–	R7	R13	–	–	–	–	LB3	97	P23
27	L1-SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	70	SHFCLK
	Pixels/Clock	8	8	16	1	1	2	2-2/3	5-1/3	2-2/3	5-1/3	8		

NOTES
[1] The 65550 also supports panel interfaces that transfer one pixel per word, but which use both edges of SHFCLK to transfer one pixel on each edge.
[2] The higher order output lines should be used when only 9 or 12 bits are needed from the 9/12/16-bit TFT interface, or when only 18 bits are needed from the 18/24-bit TFT or TFT HR interfaces. The lower order bits should be left unconnected.
[3] The 65550 controller also supports double-clock

7.26.8 Video Mode Support – Standard VGA Modes

Which super VGA Graphics modes the Chips® 65550 can support depend upon several factors, including display memory size requirements, dot clock (display pixel rate) requirements, video DRAM memory bandwidth requirement (bytes per pixel, pixel rate and bandwidth available to the CPU). For simultaneous CRT and panel operation, compatibility between panel timing requirements and CRT requirements is also a factor. The PC/II+dxe Chips® 65550 uses a 32-bit interface to 2 MB of 50 ns (typical) EDO DRAM memory. It runs at 3.3V and supports a maximum Dot Clock (DCLK) of 80 MHz. The standard VGA modes supported by the PC/II+dxe are summarized in the following table.

Table 13 VGA Standard Modes Supported

Mode# (Hex)	Display Mode	Colors	Text Display	Font Size	Pixel Res.	DotClock (MHz)	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
0, 1	Text	16	40 x 25	8x8	320x200	25.175	31.5	70
0*,1*	Text	16	40 x 25	8x14	320x350	25.175	31.5	70
0+,1+	Text	16	40 x 25	9x16	360x400	28.322	31.5	70
2,3	Text	16	80 x 25	8x8	640x200	25.175	31.5	70
2*,3*	Text	16	80 x 25	8x14	640x350	25.175	31.5	70
2+,3+	Text	16	80 x 25	9x16	720x400	28.322	31.5	70
4	Graphics	4	40 x 25	8x8	320x200	25.175	31.5	70
5	Graphics	4	40 x 25	8x8	320x200	25.175	31.5	70
6	Graphics	2	80 x 25	8x8	640x200	25.175	31.5	70
7	Text	Mono	80 x 25	9x14	720x350	25.175	31.5	70
7+	Text	Mono	80 x 25	9x16	720x400	28.322	31.5	70
D	Planar	16	40 x 25	8x8	320x200	25.175	31.5	70
D	Planar	16	80 x 25	8x8	640x200	25.175	31.5	70
F	Planar	Mono	80 x 25	8x14	640x350	25.175	31.5	70
10	Planar	16	80 x 25	8x14	640x350	25.175	31.5	70
11	Planar	2	80 x 30	8x16	640x480	25.175	31.5	60
12	Planar	16	80 x 30	8x16	640x480	25.175	31.5	60
13	Packed Pixel	256	40 x 25	8x8	320x200	25.175	31.5	70

NOTES
[1] All of the above VGA standard modes are supported directly in the Video BIOS.
[2] All VGA modes using 25.175 MHz and 28.322 MHz can also be supported using 32 MHz and 36 MHz respectively.

Table 14 Extended Resolution Modes Supported – Preliminary

Mode# (Hex)	Display Mode	Colors	Text Display	Font Size	Pixel Res.	DotClock (MHz)	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
20	4-bit Linear	16	80x30	8x16	640x480	25.175	31.5	60
20	4-bit Linear	16	80x30	8x16	640x480	31.500	37.9	72
20	4-bit Linear	16	80x30	8x16	640x480	31.500	37.5	75
22	4-bit Linear	16	100x37	8x16	800x600	36.000	35.1	56
22	4-bit Linear	16	100x37	8x16	800x600	40.000	37.9	60
22	4-bit Linear	16	100x37	8x16	800x600	50.350	48.1	72
22	4-bit Linear	16	100x37	8x16	800x600	49.500	46.9	75
24 I	4-bit Linear	16	128x48	8x16	1024x768	44.900	35.5	43
24	4-bit Linear	16	128x48	8x16	1024x768	65.000	48.4	60

Mode# (Hex)	Display Mode	Colors	Text Display	Font Size	Pixel Res.	DotClock (MHz)	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
24	4-bit Linear	16	128x48	8x16	1024x768	75.575	57.5	70
24	4-bit Linear	16	128x48	8x16	1024x768	78.750	60	75
28 I	4-bit Linear	16	128x48	8x16	1280x1024	78.750	46.433	43
28	4-bit Linear	16	128x48	8x16	1280x1024	80.000	80.0	43
30	8-bit Linear	256	80x30	8x16	640x480	25.175	31.5	60
30	8-bit Linear	256	80x30	8x16	640x480	31.500	37.9	72
30	8-bit Linear	256	80x30	8x16	640x480	31.500	37.5	75
32	8-bit Linear	256	100x37	8x16	800x600	36.000	35.1	56
32	8-bit Linear	256	100x37	8x16	800x600	40.000	37.9	60
32	8-bit Linear	256	100x37	8x16	800x600	50.350	48.1	72
32	8-bit Linear	256	100x37	8x16	800x600	49.500	46.9	75
34 I	8-bit Linear	256	128x48	8x16	1024x768	44.900	35.5	43
34	8-bit Linear	256	128x48	8x16	1024x768	65.000	48.4	60
34	8-bit Linear	256	128x48	8x16	1024x768	75.575	57.5	70
34	8-bit Linear	256	128x48	8x16	1024x768	78.750	60.00	75
40	15-bit Linear	32K	80x30	8x16	640x480	50.350	31.5	60
40	15-bit Linear	32K	80x30	8x16	640x480	63.000	37.9	72
40	15-bit Linear	32K	80x30	8x16	640x480	63.000	37.5	75
41	16-bit Linear	64K	80x30	8x16	640x480	50.350	31.5	60
41	16-bit Linear	64K	80x30	8x16	640x480	63.000	37.9	72
41	16-bit Linear	64K	80x30	8x16	640x480	63.000	37.5	75
42	15-bit Linear	32K	100x37	8x16	800x600	72.000	35.1	56
42	15-bit Linear	32K	100x37	8x16	800x600	80.000	37.9	60
43	16-bit Linear	64K	100x37	8x16	800x600	72.000	35.1	56
43	16-bit Linear	64K	100x37	8x16	800x600	80.000	37.9	60
50	24-bit Linear	16M	80x30	8x16	640x480	75.525	31.5	60
60	Text	16	132x25	8x16	1056x400	41.500	31.5	70
61	Text	16	132x50	8x8	1056x400	41.500	31.5	70
6A/70	Planar	16	100x37	8x16	800x600	36.000	35.1	56
6A/70	Planar	16	100x37	8x16	800x600	40.000	37.9	60
6A/70	Planar	16	100x37	8x16	800x600	50.350	48.1	72
6A/70	Planar	16	100x37	8x16	800x600	49.500	46.9	75
72 I/72 I	Planar	16	128x48	8x16	1024x768	44.900	35.5	43
72/75	Planar	16	128x48	8x16	1024x768	65.000	48.4	60
72 I/72 I	Planar	16	128x48	8x16	1024x768	75.525	57.5	70
72/75	Planar	16	128x48	8x16	1024x768	78.750	60.0	75
78	Packed Pixel	256	80x25	8x16	640x400	25.175	31.5	70
79	Packed Pixel	256	80x30	8x16	640x480	25.175	31.5	60
79	Packed Pixel	256	80x30	8x16	640x480	31.500	37.9	72
79	Packed Pixel	256	80x30	8x16	640x480	31.500	37.5	75
7C	Packed Pixel	256	100x37	8x16	800x600	36.000	35.1	56
7C	Packed Pixel	256	100x37	8x16	800x600	40.000	37.9	60
7C	Packed Pixel	256	100x37	8x16	800x600	50.350	48.1	72
7C	Packed Pixel	256	100x37	8x16	800x600	49.500	46.9	75
7E I	8-bit Linear	256	128x48	8x16	1024x768	44.900	35.5	43
7E	8-bit Linear	256	128x48	8x16	1024x768	65.000	48.4	60
7E	8-bit Linear	256	128x48	8x16	1024x768	75.525	57.5	70
7E	8-bit Linear	256	128x48	8x16	1024x768	78.750	60.00	75

NOTES
[1] *"I" modes are interlaced.*

7.26.9 Video Resolution, Colors, Refresh & Clocks Support – CRT, & TFT Panels

Resolution and Color Depth supported for CRT displays and/or TFT panels are contained in this section. In the following table, a representative list of the most memory bandwidth intensive resolution and color depth combinations and of the maximum screen refresh frequencies is provided. The table applies for both CRT and TFT panels, including simultaneous CRT and TFT operation. This list is not a complete list of all modes that the VGA BIOS can support. Refer to the Chips VGA BIOS documentation for more information above VGA BIOS mode support.

Table 15 Video Resolution, Colors, Refresh, & Clocks Support – CRT, & TFT Panels

Resolution and Color Depth [1]	Screen Refresh [2]	Horiz. Freq.	Dot Clock	Notes
640 x 480 x 8 bpp	85 Hz	43.3 KHz	36 MHz	
640 x 480 x 16 bpp	85 Hz	43.3 KHz	36 MHz	
640 x 480 x 24 bpp	85 Hz	43.3 KHz	36 MHz	
800 x 600 x 8 bpp	85 Hz	53.7 KHz	56.25 MHz	
800 x 600 x 16 bpp	85 Hz	53.7 KHz	56.25 MHz	
800 x 600 x 24 bpp	60 Hz	37.9 KHz	40 MHz	[3]
1024 x 768 x 8 bpp	85 Hz	68.7 KHz	94.5 MHz	
1024 x 768 x 16 bpp	56 Hz	45.2 KHz	60.7 MHz	[3]
1280 x 1024 x 8 bpp	60 Hz	64 KHz	108 MHz	

NOTES

[1] Table contents provided by the document, "Chips HiQVideo Series Mode Support", Application Note AN89, Revision 1.4, Feb 1996. Refer to the document for a list that includes all combinations supported. Except for the interlaced modes in this table, all modes apply to both CRT displays and to TFT panels, including simultaneous CRT and TFT operation.

[2] This is the maximum supported Screen Refresh frequency for the corresponding Resolution and Color Depth

[3] Mode slightly exceeds the computed bandwidth of the main display memory. However, the mode may still be supported depending on final silicon characterization and testing. Support may be possible with second-order software adjustments in the programming of the internal registers and/or somewhat reduced memory bandwidth available for CPU accesses.

7.26.10 Video Resolution, Colors, and Refresh Support – STN-DD Panels

In the following tables, a representative list of the most memory bandwidth intensive resolution and color depth combinations and of the maximum screen refresh frequencies is provided for each STN-DD panel type. Video overlay does not apply to the PC/II+dxe video interface. See notes for support of simultaneous CRT & panel operation. This list is not a complete list of all modes that the VGA BIOS can support – please refer to the Chips VGA BIOS documentation for more information above VGA BIOS mode support.

Table 16 Video Resolution, Colors & Refresh Support – STN-DD Panels

Resolution and Color Depth [1]	Screen Refresh					
	640x480 Color	640x480 Mono	800x600 Color	800x600 Mono	1024x768 Color	1024x768 Mono
640 x 480 x 8 bpp	75 Hz	75 Hz	75 Hz	75 Hz	70 Hz	70 Hz
640 x 480 x 16 bpp	85 Hz	75 Hz	75 Hz	75 Hz	70 Hz [4]	70 Hz
640 x 480 x 24 bpp	75 Hz [3]	75 Hz	75 Hz [3,4]	75 Hz [3,4]	70 Hz [5]	70 Hz [5]
800 x 600 x 8 bpp	75 Hz	75 Hz	85 Hz	75 Hz	70 Hz [3]	70 Hz
800 x 600 x 16 bpp	75 Hz	75 Hz	85 Hz [4]	75 Hz [3]	70 Hz [3,4]	70 Hz [3,4]
800 x 600 x 24 bpp	75 Hz [3]	75 Hz	85 Hz [5]	75 Hz [5]	70 Hz [3,5]	70 Hz [5]
1024 x 768 x 8 bpp	75 Hz	75 Hz	75 Hz	75 Hz	70 Hz [5]	70 Hz
1024 x 768 x 16 bpp	75 Hz	75 Hz	75 Hz [4]	75 Hz [3]	70 Hz [5]	70 Hz [5]
1280 x 1024 x 8 bpp	75 Hz	75 Hz	75 Hz	75 Hz	70 Hz [5]	70 Hz

NOTES

[1] Table contents provided by the document, "Chips HiQVideo Series Mode Support", Application Note AN89, Revision 1.4, Feb 1996. Refer to the document for a list that includes all combinations supported. Unless otherwise noted (see [4,5]), simultaneous CRT and STN-DD panel operation is supported.

[2] This is the maximum supported Screen Refresh frequency for the corresponding Resolution and Color Depth

[3] Mode slightly exceeds the computed bandwidth of the main display memory. However, the mode may still be supported depending on final silicon characterization and testing. Support may be possible with second-order software adjustments in the programming of the internal registers and/or somewhat reduced memory bandwidth available for CPU accesses.

[4] Simultaneous CRT and panel operation is not supported. Panel-only operation can be supported (see note [5] below).

[5] For panels, graphics raster registers and DCLK must be programmed for half the specified refresh rate, and frame acceleration must be enabled to achieve the specified panel FLM frequency. Simultaneous operation with a CRT is not supported.

[6] STN-DD panels require additional buffering compared to TFT panels and CRT displays. STN-DD panels usually are divided into upper and lower half-panels, which must be refreshed simultaneously. A "DD" buffer allows pixels to be read from display memory in a single-scan manner while refreshing the STN-DD panel in a dual-drive ("DD") manner. In the PC/II+dxe, the DD buffer is embedded in the main display memory in an off-screen area. In this case, the DD buffer can be either full-frame or half-frame. With a half-frame DD buffer, the refresh rate of the STN-DD panel (FLM frequency) is double the refresh rate of the CRT. This doubling effect is also referred to as frame acceleration. In all of the STN-DD mode listed, frame acceleration can be used to achieve a panel refresh rate twice as high as the specified refresh rate, except in cases where frame acceleration is already assumed to be enabled.

7.27 Watchdog & Power Monitor

The PC/II+dxe contains a DS1706S Microprocessor Supervisor that provides a Watchdog timer. The Watchdog WDS# output is tied to RST# causing a minimum 130 microsecond CPU reset to occur when the watchdog timer triggers. A jumper (JP01) is included between WDS# and RST# to permanently disable the watchdog function (remove jumper to disable Watchdog, install jumper to enable watchdog function).

The Watchdog input must be driven low periodically, at a ***minimum rate of once per second***, to prevent the watchdog WDS# output from being activated. This strobe is normally driven by the PC/II+dxe board hardware, and in this mode, the watchdog does not trigger, and the Watchdog timer is in inactive mode.

To allow the Watchdog timer to trigger and cause a CPU reset, the Watchdog jumper must be inserted, the Watchdog must be activated, and the Watchdog strobe must not have been issued for a duration of 1 second.

A program-accessible interface to the Watchdog Enable/Disable control signal and the Watchdog Strobe signal are provided by the PC/II+dxe BIOS, using software interrupt 15h, functions 0FEh and 0FDh.

1. FUNCTION 0FEh – ACTIVATE AND DEACTIVATE WATCHDOG TIMER

This function activates the watchdog timer to allow software control of strobing, or deactivates the watchdog timer to disable watchdog functionality.

In ACTIVE mode the watchdog will trigger and cause a CPU reset if the watchdog jumper is inserted and a software strobe has not been issued to the watchdog in the last second using function 0FDh. Therefore, strobing at a one strobe per second rate or faster is required.

In INACTIVE mode strobing is not required and the watchdog will **not** cause a CPU reset to occur. This is the default at boot time.

```
MOV    AH,0FEh
MOV    AL,<Command>                    00h = ACTIVATE watchdog
                                       01h = DEACTIVATE watchdog
INT    15h
-- returns here after the specified watchdog MODE has been entered
       / ALL Registers are preserved
```

2. FUNCTION 0FDh – STROBE WATCHDOG TIMER

This function strobes the watchdog timer, causing its timer to restart. In ACTIVE mode (see function 0FEh), the watchdog must be strobed at a one strobe per second rate, and preferably at a faster rate, to prevent the watchdog timer from expiring and a CPU reset from occurring. In INACTIVE mode this function has no affect.

```
MOV    AH,0FDh
INT    15h
-- returns here after one strobe has been issued to the watchdog
       / ALL Registers are preserved
```

8 System Resource Maps

8.1 I/O Address Map

Table 17 I/O Map

I/O ADDRESS REGION [1]	USED BY	DESCRIPTION	USED FOR
0000-000F	ACC2089	DMA controller 1	8237A-5
0020-0021	ACC2089	Interrupt controller 1	8259A-MASTER
0040-0043	ACC2089	Timer	8254
0060,0064	ACC2089	Keyboard controller	
0070-0071	ACC2089	Real-time clock, NMI mask	DS1685
0080-008F	ACC2089	DMA page register	74LS612
0092	ACC2089	Alternate gate a20, fast reset register	
00A0-00A1	ACC2089	Interrupt controller 2	8259A-SLAVE
00C0-00DF	ACC2089	DMA controller 2	8237A-5
00F0	ACC2089	Clear math coprocessor busy	
00F1	ACC2089	Reset math coprocessor	
00F2	ACC2089	ACC2089 configuration register index	BIOS
00F3	ACC2089	ACC2089 configuration register data	BIOS
00F8-00FF	ACC2089	Math coprocessor	
0102	65550	VGA global enable	
0140-015F	SCSI	SCSI-2 controller – primary	Scsi I/O
0180-019F	CPLD	Reserved	
01F0-01F7	ACC2089	Primary HDC	IDE
02F8-02FF	ACC2089	COM2-IRQ3	Serial I/O – #2
0300-030F	CS8900	Ethernet controller	Ethernet
0340-035F	SCSI	SCSI-2 controller – secondary	Scsi I/O
0370-0377	ACC2089	Secondary FDC	
0378-037A	ACC2089	LPT1 (Standard mode)	Printer #1
037B-037F	ACC2089	LPT1 (EPP mode)	Printer #1 – EPP
03B4-03B5	65550	VGA crtc index / data	VGA BIOS
03BA	65550	VGA status register / Feature Control Register	VGA BIOS
03C0-03C1	65550	VGA attrib controller index / data	VGA BIOS
03C2	65550	VGA input status register 0 / MSR	VGA BIOS
03C3	65550	VGA motherboard video system enable	VGA BIOS
03C4-03C5	65550	VGA sequence index / data	VGA BIOS
03C6-03C9	65550	VGA color palette registers	VGA BIOS
03CA	65550	VGA feature control register	VGA BIOS
03CC	65550	VGA misc output register	VGA BIOS
03CE-03CF	65550	VGA graphics controller index/data	VGA BIOS
03D0-03D1	65550	Video flat panel extension regs index/data	VGA BIOS
03D2-03D3	65550	Video multimedia extension regs index/data	VGA BIOS

I/O ADDRESS REGION [1]	USED BY	DESCRIPTION	USED FOR
03D4-03D5	65550	VGA CRTC index/data (CGA emulation)	VGA BIOS
03D6-03D7	65550	Video configuration extensions data/index	VGA BIOS
03DA	65550	VGA status register	VGA BIOS
03F0-03F7	ACC2089	Primary FDC	Floppy
03F8-03FF	ACC2089	COM1-IRQ4	Serial I/O – #1
0778-077A	ACC2089	LPT (ECP mode)	Printer #1 – ECP

NOTES
[1] Addresses are expressed in hexadecimal notation; all addresses are in the 64K physical I/O address space supported by the processor.

8.2 Memory Map

Table 18 Memory Map

MEMORY ADDRESS REGION [1]	LENGTH	DESCRIPTION
00000 – 9FFFF	640K	Base Memory Address Region.
A0000 – AFFFF	64K	Video 65550 – VGA Frame Buffer
B0000 – B7FFF	32K	Video 65550 – MDA Emulation Character Buffer
B8000 – BFFFF	32K	Video 65550 – CGA Emulation Frame Buffer
C0000 – CFFFF	64K	Option BIOS Memory Address Region. This memory address region is ALWAYS shadowed. All memory accesses to this region are always forwarded to system memory, never to the system bus. This region typically contains the VGA BIOS.
D0000 – DFFFF	64K	Flash Array Memory Address Region (for accessing any 1 of 128 – 64K flash sectors). This memory address region is used to access both User Flash pages and Bios Flash pages. It can be shadowed with system memory when access to Flash is not required. Memory accesses are forwarded to the system bus, causing FCS (Flash Chip Select) to be asserted, only if the Flash Window is enabled The page numbers are assigned as follows: page 0 – 127 User flash array page 128 – 131 BIOS flash
E0000 – E7FFF	32K	Reserved.
E8000 – EFFFF	32K	Flash Disk (Disk-on-Chip) Memory Address Region. This memory address region is used to access the Disk-On-Chip, and it can be shadowed with system memory when access to Disk-On-Chip is not required. Memory accesses are forwarded to the system bus, causing X32CS# (Disk-on-Chip Chip Select) to be asserted only if X32CS is enabled.
F0000 – FFFFF	64K	BIOS ROM Memory Address Region. This memory address region is used for standard BIOS ROM. Memory write accesses to this address region are always forwarded to system memory, never to the system bus. Memory read accesses to this address region are forwarded to the system bus, only if enabled, otherwise they are forwarded to system memory.

NOTES
[1] Addresses are expressed in hexadecimal notation; all addresses are in the first 1 MB of physical address space (also known as 'real memory' address region).

8.2.1 Memory Shadowing

Memory shadowing is normally automatically performed by the PC/II+dxe BIOS. At the hardware level, the Shadowing options for EDO DRAM are controlled by register 0x02 in the ACC2089. Shadowing hardware options are described below; please refer to the ACC2089 data sheet for further details.

8.2.2 Shadow Disable

After a power-up or a system reset, all shadowing is disabled. Therefore any memory accesses to the area from 0x000C0000 – 0x000FFFFF is directed to the system bus.

8.2.3 Shadow Enable

Shadowing may be enabled on a 64K-page basis for each of the 64 KB pages beginning at 0x000C0000, 0x000D0000, 0x000E0000 and 0x000F0000. When shadowing is enabled, both read and write operations are directed to DRAM rather than to the system bus.

8.2.4 Shadow Protection

In addition, there is a single write-enable bit, which can inhibit write operations to shadow RAM. If a memory region is not shadowed, then both read and write operations are forwarded to the bus. Both U040, the X-32 Flash Disk (Disk-on-Chip®) device, and U021, the Flash Array device, have enable bits that allow the corresponding chip select to be disabled.

8.3 Interrupt IRQ Map

Table 19 Interrupt Map

INTERRUPT REQUEST NUMBER [1,2]	SOURCE	DESCRIPTION
IRQ0	ACC2089	TIMER 0
IRQ1	ACC2089	KEYBOARD
IRQ2	ACC2089	Cascade to Interrupt Controller 2
IRQ3	ACC2089	COM2
IRQ4	ACC2089	COM1
IRQ5	CS8900	ETHERNET
IRQ6	ACC2089	FDC
IRQ7	ACC2089	LPT1
IRQ8	DS1685	Real Time Clock – Timer/Alarm
IRQ9	CPLD	COM4
IRQ10	CS8900	ETHERNET– Default
IRQ11	SCSI	SCSI
IRQ11	CS8900	ETHERNET
IRQ12	ACC2089	PS/2 MOUSE
IRQ13	-	(Numeric Coprocessor)
IRQ14	ACC2089	IDE
IRQ15	-	-

NOTES
[1] Interrupt request numbers are enumerated from 0 through 15 per the conventional AT standard. Interrupt request levels are numbered 0 through 7 in each physical 8259A interrupt controller. The interrupt controllers are tied together through interrupt level 2 of control #1 (that is, interrupt pending requests are presented from interrupt controller #2 to level 2 of interrupt controller #1). The physical implementation of interrupt controllers is internal to the ACC 2089. This implementation mirrors the implementation of two 8259A controllers, so that the interface is identical to the AT standard. When an interrupt is pending for IRQ8-IRQ15, the interrupt is in-service in both controllers, in controller #1 at level 2, and controller #2 at level 0-7; both controllers are normally acknowledged after service completes to clear the pending interrupt, per the standard AT standard.
[2] The IRQ's listed in this table are assigned for use by the indicated source by default. Users have the option of changing these default assignments using either a Plug and Play aware operating system (such as Windows for example) or using a DOS based Megatel Utility that can be obtained from Megatel; for more information, please contact Megatel Engineering.

8.4 DMA Channel Map

Table 20 DMA Map

DMA REQUEST NUMBER [1]	SOURCE	DESCRIPTION
DRQ0		
DRQ1		
DRQ2	ACC2089	Floppy Disk Controller
DRQ3		
DRQ4	ACC2089	Cascade for DMA Controller 1
DRQ5		
DRQ6	SCSI	SCSI-2 Controller
DRQ7		

NOTES
[1] DMA request numbers are enumerated from 0 through 7 per the conventional AT standard. Two DMA controllers, the first containing four 8-bit channels (0-3 – DRQ0-DRQ3) is cascaded to channel 0 of the second controller (DRQ4). Controller #2 contains four 16-bit channels.

9 Connector Pinouts

This section contains pinout and signal description details for each connector on the PC/II+dxe.

These connectors are described,

J001 – Fan Connector – 1x2 1.25 mm Molex
J002 – Alternate Video 24-Bit Panel Connector – 2x18 Header
J003 – Alternate +3.3V Power Connector – 1x5 Pin Header
J901 – Peripheral I/O Connector (96-Pin Eurocard DIN)
- J901 Peripheral I/O – Power & Ground
- J901 Peripheral I/O – Serial COM1
- J901 Peripheral I/O – Serial COM2
- J901 Peripheral I/O – Serial COM4
- J901 Peripheral I/O – Floppy Disk
- J901 Peripheral I/O – Keyboard Interface
- J901 Peripheral I/O – Reset Interface
- J901 Peripheral I/O – PC Speaker Output Interface
- J901 Peripheral I/O – Parallel Port LPT1 Interface
- J901 Peripheral I/O – SCSI Bus Interface
- J901 Peripheral I/O – Video Analog (CRT–VGA) Interface
- J901 Peripheral I/O – Video Panel (8/16 Bit) Interface

J902 – ISA Bus Connector – 8 Bit
J903 – Ethernet Connector (2x5 .100 Inch Header)
J904 – IDE Connector (2x22 2mm Header)
J905 – ISA Bus Extension Connector – 16-Bit (I/O)
J906 – Alternate +5V Power Connector – 1x12 Pin Header
JP05 – Mouse Connector – 1x2 Pin Header

9.1 J001 – Fan Connector – 1x2 1.25 mm Molex

This connector is optional. It provides power only for an optional Cpu fan. The use of a Cpu fan is dependent upon the environment in which the PC/II+dxe is operating, and the speed at which the processor has been strapped.

Table 21 Signals – J001 – Fan Connector 1x2 1.25 mm Molex

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
+5V	A1	+5V	+5v
GND	A2	GND	Ground

9.2 J002 – Alternate Video 24-Bit Panel Connector – 2x18 Header

This connector is an option for the PC/II+dxe. If used, all of the panels and modes supported by the Chips 65550 video controller can be used with this board.

Note – the compatible video interface available on J901 (the 96-pin DIN connector) supports panels and modes provided by the Chips 65530 video controller (a predecessor to the 65550). Only one panel can be attached to the PC/II+dxe regardless of which interface is used. For a description of the 8/16-bit panels supported by J901 (96-pin DIN connector), please refer to section 0 on page 77.

Table 22 Pinout – J992 – Full 24-Bit Panel Interface Header

PIN NAME [1]	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
GND	1	Ground	Ground
+5V	2	+5V	POWER +5V
L1-FPD23	3	Data Output P23	Flat panel data output P23. Active high. Output.
L1-FPD22	4	Data Output P22	Flat panel data output P22. Active high. Output.
L1-FPD21	5	Data Output P21	Flat panel data output P21. Active high. Output.
L1-FPD20	6	Data Output P20	Flat panel data output P20. Active high. Output.
L1-FPD19	7	Data Output P19	Flat panel data output P19. Active high. Output.
L1-FPD18	8	Data Output P18	Flat panel data output P18. Active high. Output.
L1-FPD17	9	Data Output P17	Flat panel data output P17. Active high. Output.
L1-FPD16	10	Data Output P16	Flat panel data output P16. Active high. Output.
L1-FPD15	11	Data Output P15	Flat panel data output P15. Active high. Output.
L1-FPD14	12	Data Output P14	Flat panel data output P14. Active high. Output.
L1-FPD13	13	Data Output P13	Flat panel data output P13. Active high. Output.
L1-FPD12	14	Data Output P12	Flat panel data output P12. Active high. Output.
L1-FPD11	15	Data Output P11	Flat panel data output P11. Active high. Output.
L1-FPD10	16	Data Output P10	Flat panel data output P10. Active high. Output.
L1-FPD9	17	Data Output P9	Flat panel data output P9. Active high. Output.
L1-FPD8	18	Data Output P8	Flat panel data output P8. Active high. Output.
L1-FPD7	19	Data Output P7	Flat panel data output P7. Active high. Output.
L1-FPD6	20	Data Output P6	Flat panel data output P6. Active high. Output.
L1-FPD5	21	Data Output P5	Flat panel data output P5. Active high. Output.
L1-FPD4	22	Data Output P4	Flat panel data output P4. Active high. Output.
L1-FPD3	23	Data Output P3	Flat panel data output P3. Active high. Output.
L1-FPD2	24	Data Output P2	Flat panel data output P2. Active high. Output.
L1-FPD1	25	Data Output P1	Flat panel data output P1. Active high. Output.
L1-FPD0	26	Data Output P0	Flat panel data output P0. Active high. Output.
L1-SHFCLK	27	Shift Clock	(SHFCLK or CL2 or SHFCLKL) This signal is the pixel clock for flat panel data. Active high. Output.
L1-LP	28	Latch Pulse	Flat Panel equivalent of HSYNC. Active high. Output.

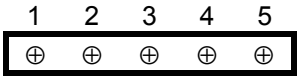
PIN NAME [1]	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
L1-FLM	29	First Line Marker	Flat Panel equivalent of VSYNC. Active high. Output.
L1-M	30	M signal	This signal is the M-signal for panel AC drive control (may also be called ACDCLK). May also be configured as BLANK# or as Display Enable (DE) for TFT Panels. Active High. Output.
L1-ENAVEE	31	Enable VEE	(ENAVEE or ENABKL) Power sequencing controls for panel LCD bias voltage VEE, I/O. The polarity of this signal can be selected by option "n" - either active low or active high.
L1-ENAVDD	32	Enable VDD	Power sequencing controls for panel driver electronics voltage VDD. I/O.
L1-ENABKL	33	Enable Backlight	(ENBKL or A27 or GP1 or DCLK or CS) This signal is the Enable Backlight output signal. It may be configured for other functions (see Chips 65550 Datasheet – Extension Registers FR0C and FR0F and pin descriptions of MCD0-15 and A26/A27 for more information). (Chips Revision 1.5 10/14/97 65550 Subject to Change without Notice). I/O.
L1-ACTI	34	Activity Indicator	(ACTI or A26 or GP0 or DDAT or CS) This signal is the Activity Indicator output. It may be configured for other functions (see Chips 65550 Datasheet – Extension Registers FR0C and FR0F and pin descriptions of MCD0-15 and A26/A27 for more information). I/O.
GND	35	Ground	Ground
+5V	36	+5V	POWER +5V

NOTES
[1] *The Pin Name is derived from the directly-attached 65550 source signal name.*

9.3 J003 – Alternate +3.3V Power Connector – 1x5 Pin Header

Version 2.03 and higher of the PC/II+dxe allows the on-board +3.3v requirements to be supplied from an external user +3.3v 5% power supply (it may also be supplied using one of the on-board regulator options). When the External +3.3v Power option is chosen, the Alternate +3.3v Power Connector (J003) is populated on the board, and J003 then supplies the +3.3v 5% voltage to the board.

Figure 4 Diagram – Alternate +3.3v Power Header J003 – 1x5 PIN .100" R/A Male Header



NOTES
1 Top (component) view is shown.

Table 23 Pinout – Alternate +3.3v Power J003 – 1x15 PIN .100" R/A Male Header

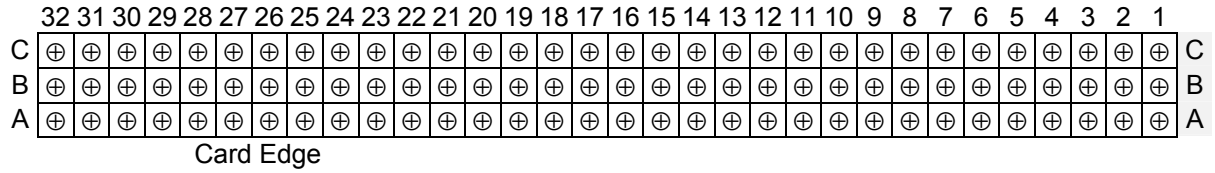
PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
+3.3V	1	+3.3V	+3.3v 5% sourced by off-board supply
GND/KEY	2	GND/KEY	Ground (or Key)
GND	3	GND	Ground
GND	4	GND	Ground
+3.3V	5	+3.3V	+3.3v 5% sourced by off-board supply

9.4 J901 – Peripheral I/O Connector (96-Pin Eurocard DIN)

This connector supplies power (+5V) to the Cpu board, and provides a peripheral interface to the following devices: Video Analog (CRT) or 8/16-bit Panel, two Serial ports, Parallel port, Keyboard, Floppy Disk, Printer, SCSI bus, Reset switch, and PC Speaker. Other on-board I/O is pulled to separate on-board connectors.

The Peripheral I/O connector pad area is a 3x32 .100 inch grid which can be populated with headers or connectors, one of those specified in this document or by the customer. Typically, the PC/II+dxe is shipped with the Eurocard DIN (type C) 96-pin 3-row right-angle male connector.

Figure 5 Diagram – Peripheral I/O J901 (Rows A,B, and C) – 3X32 .100 Eurocard DIN Connector



NOTES
[1] Top (component) view is shown. This is the view when facing a either a straight connector from the top, or a right-angle connector facing the outer side (the mating side).

Table 24 Pinout – Peripheral I/O J901 (Rows A, B, C) – 3 x 32 Eurocard DIN Connector

POS	ROW C	ROW B	ROW A
1	GND	+5V	VID-P3
2	VID-FRM V1-VSYNC	VID-P0	VID-P5
3	VID-LP V1-HSYNC	VID-P1	VID-P8
4	VID-P9 V1-G	VID-P2	VID-SCK
5	VID-P4	GND	VID-M
6	VID-P7	VID-P6	VID-P10 V1-B
7	C1-RI	C2-RI	VID-P11 V1-R
8	C1-DTR	C2-DTR	RESERVED
9	C1-CTS	C2-CTS	PC-SPKROUT
10	C1-TXD	C2-TXD	P1-SLCT
11	C1-RTS	C2-RTS	P1-PE
12	C1-RXD	C2-RXD	P1-BUSY
13	C1-DSR	C2-DSR	P1-AKN#
14	C1-DCD	C2-DCD	P1-D7
15	F1-DKCHG#	C4-RXD	P1-D6
16	F1-HDSEL#	C4-TXD	P1-D5
17	F1-RDATA#	K1-DAT	P1-D4
18	F1-WP#	K1-CLK	P1-D3
19	F1-TRK0#	P1-SLIN#	P1-D2
20	F1-WGATE#	P1-INIT#	P1-D1
21	F1-WDATA#	P1-ERR#	P1-D0
22	F1-STEP#	P1-AFD#	P1-STB#
23	F1-DIR#	S1-ATN#	S1-D0#
24	F1-MTR1#	S1-BSY#	S1-D1#
25	F1-DS0#	S1-AKN#	S1-D2#
26	F1-DS1#	S1-RST#	S1-D3#
27	F1-MTR0#	S1-MSG#	S1-D4#
28	F1-INDEX#	S1-SEL#	S1-D5#
29	GND	S1-C/D#	S1-D6#
30	RESERVED	S1-REQ#	S1-D7#
31	F1-DENSL0#	S1-I/O#	S1-DP#
32	GND	+5V	PC-RSTSW#

NOTES

9.4.1 J901 Peripheral I/O – Power & Ground

Table 25 Signals – Peripheral I/O J901 – Power & Ground

PIN NAME [1]	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
+5V	B1	+5V	Power +5v
+5V	B32	+5V	Power +5v
GND	C1	Ground	Ground
GND	B5	Ground	Ground
GND	C29	Ground	Ground
GND	C32	Ground	Ground

NOTES
[1] *See also J906 and J003 descriptions.*

9.4.2 J901 Peripheral I/O – Serial COM1

Table 26 Signals – Peripheral I/O J901 – Serial COM1 Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
C1-CTS	C9	Clear to Send	This active low input is the handshake signal which notifies the UART that the modem is ready to receive data.
C1-DCD	C14	Data Carrier Detect	This active low input is a handshake signal which notifies the UART that carrier signal is detected by the modem.
C1-DSR	C13	Data Set Ready	This active low input is the handshake signal which notifies the UART that the modem is ready to establish the communication link.
C1-DTR	C8	Data Terminal Ready	This active low output is the handshake output signal that signifies to modem that the UART is ready to establish data communication link.
C1-RI	C7	Ring Indicator	This active low input is the handshake signal which notifies the UART that the telephone ring signal is detected by the modem.
C1-RTS	C11	Request to Send	This Active low output is the handshake output signal that notifies the modem that the UART is ready to transmit data. The hardware reset will clear the RTS signal to inactive mode (high).
C1-RXD	C12	Receive Data	This input is the receive data serial input line, which carries RS-232 data.
C1-TXD	C10	Transmit Data	This output is the transmit data serial output line, which carries RS-232 data.

9.4.3 J901 Peripheral I/O – Serial COM2

Table 27 Signals – Peripheral I/O J901 – Serial COM2 Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
C2-CTS	B9	Clear to Send	This active low input is the handshake signal which notifies the UART that the modem is ready to receive data.
C2-DCD	B14	Data Carrier Detect	This active low input is a handshake signal which notifies the UART that carrier signal is detected by the modem.
C2-DSR	B13	Data Set Ready	This active low input is the handshake signal which notifies the UART that the modem is ready to establish the communication link.
C2-DTR	B8	Data Terminal Ready	This active low output is the handshake output signal that signifies to modem that the UART is ready to establish data communication link.
C2-RI	B7	Ring Indicator	This active low input is the handshake signal which notifies the UART that the telephone ring signal is detected by the modem.
C2-RTS	B11	Request to Send	This Active low output is the handshake output signal that notifies the modem that the UART is ready to transmit data. The hardware reset will clear the RTS signal to inactive mode (high).
C2-RXD	B12	Receive Data	This input is the receive data serial input line, which carries RS-232 data.
C2-TXD	B10	Transmit Data	This output is the transmit data serial output line, which carries RS-232 data.

9.4.4 J901 Peripheral I/O – Serial COM4

Table 28 Signals – Peripheral I/O J901 – Serial COM4 Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
C4-RXD	B15	Receive Data	This input is the receive data serial input line, which carries RS-232 data.
C4-TXD	B16	Transmit Data	This output is the transmit data serial output line, which carries RS-232 data.

9.4.5 J901 Peripheral I/O – Floppy Disk

Table 29 Signals – Peripheral I/O J901 – Floppy Disk Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
F1-DENSL0#	C31	Density Select	This signal, used with dual speed drives, when active low, reduces the spindle speed, nominally from 360rpm to 300rpm.
F1-DIR#	C23	Direction	This active low output determines the direction of the head movement (low = step-in, high = step-out). During the write or read modes, this output is high.
F1-DKCHG#	C15	Disk Change	This disk interface input indicates when the disk drive door has been opened. This active-low signal is read from bit D7 of address xx7h.
F1-DS0#	C25	Drive Select 0	Active low, output selects drive 0.
F1-DS1#	C26	Drive Select 1	Active low, output selects drive 1.
F1-HDSEL#	C16	Head Select	This active low output determines which disk drive head is active. Low = Head 0, high (open) = Head 1.
F1-INDEX#	C28	Index Status	This active low input signal senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
F1-MTR0#	C27	Motor On 0	Active-low output selects motor drive 0 (1st drive).
F1-MTR1#	C24	Motor On 1	Active-low output selects motor drive 1 (2nd drive).
F1-RDATA#	C17	Read Serial Data	This active-low, raw data read signal from the disk is connected here. Each falling edge represents a flux transition of the encoded data.
F1-STEP#	C22	Step Head	This active low output signal produces a pulse at a software-programmable rate to move the head during a seek operation.
F1-TRK0#	C19	Track 00	This active low input signal senses from the disk drive that the head is positioned over the outermost track.
F1-WDATA#	C21	Write Serial Data	This active low output is a write-precompensated serial data to be written onto the selected disk drive. Each falling edge causes a flux change on the media.
F1-WGATE#	C20	Write Gate	This active-low, high-drive output enables the write circuitry of the selected disk drive. This signal prevents glitches during power-up and power-down. This prevents writing to the disk when power is cycled.
F1-WP#	C18	Write Protected Status	This active-low input signal senses from the disk drive that a disk is write-protected. Any write command is ignored.

9.4.6 J901 Peripheral I/O – Keyboard Interface

Table 30 Signals – Peripheral I/O J901 – Keyboard Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
K1-CLK	B18	Keyboard Clock	This output is the keyboard interface clock.
K1-DAT	B17	Keyboard Data	This input is the keyboard serial data line.

9.4.7 J901 Peripheral I/O – Reset Interface

Table 31 Signals – Peripheral I/O J901 – Reset Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
PC-RSTSW#	A32	Manual Reset	Hard Reset Input, Active low. This signal drives the Manual-Reset Input. An internal 10kΩ pull-up resistor (typical) is provided on this signal line. Leave open if unused. Reset remains asserted as long as this signal is held low and for 200ms (typical; minimum 140ms) after this signal is floated. This input should be driven to Ground to activate the on-board Reset, and left open or pulled high to de-activate the on-board Reset. This input line is +5V tolerant and can be driven with a TTL input. The Reset threshold is set to 0.75V (± 10%).

9.4.8 J901 Peripheral I/O – PC Speaker Output Interface

Table 32 Signals – Peripheral I/O J901 – PC Speaker Output Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
PC-SPKROUT	A9	Speaker Output	This signal is used to control the Speaker Output and should connect to the Speaker.

9.4.9 J901 Peripheral I/O – Parallel Port LPT1 Interface

Table 33 Signals – Peripheral I/O J901 – Parallel LPT1 Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
P1-AFD#	B22	Autofeed Output	This active low output causes the printer to feed one line after each line is printed. This signal is the complement of Printer Control Reg bit 1.
P1-AKN#	A13	Acknowledge	This active low output from the printer indicates it has received the data and is ready to accept new data. Printer Status Reg. Bit 6 reads the PACK# input.
P1-BUSY	A12	Busy	This signal indicates the status of the printer. A high indicates the printer is busy and not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input.
P1-D0	A21	Port Data – Bit0	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D1	A20	Port Data – Bit1	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D2	A19	Port Data – Bit2	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D3	A18	Port Data – Bit3	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D4	A17	Port Data – Bit4	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D5	A16	Port Data – Bit5	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D6	A15	Port Data – Bit6	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-D7	A14	Port Data – Bit7	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-ERR#	B21	Error	This active low signal indicates an error condition at the printer.
P1-INIT#	B20	Initiate Output	This active low signal is bit 2 of the printer control register. This is used to initiate the printer when low.
P1-PE	A11	Paper End	This signal indicates that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input.
P1-SLCT	A10	Printer Selected Status	This active high output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input.
P1-SLIN#	B19	Printer select input	This active low signal selects the printer. This is the complement of bit 3 of the Printer Control Register.
P1-STB#	A22	Strobe Output	This active low pulse is used to strobe the printer data into the printer. This output signal is the complement of bit 0 of the Printer Control Register.

9.4.10 J901 Peripheral I/O – SCSI Bus Interface

Table 34 Signals – Peripheral I/O J901 – SCSI Bus Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
S1-AKN#	B25	Acknowledge	A signal driven by an initiator to indicate an acknowledgment for a REQ/ACK data transfer handshake.
S1-ATN#	B23	Attention	A signal driven by an initiator to indicate the ATTENTION condition.
S1-BSY#	B24	Busy	An "OR-tied" signal that indicates that the bus is being used. It may be driven by all SCSI devices that are actually arbitrating during Arbitration, driven by the initiator, target or both during Selection & Reselection, or driven by the target during all other phases.
S1-C/D#	B29	Control/Data	A signal driven by a target that indicates whether CONTROL or DATA information is on the DATA BUS. True indicates CONTROL.
S1-D0#	A23	Data Bus Bit Signal 0	Data bit signal 0. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. S1-D1# thru S1-D8# define eight data-bit signals. Together with the S1-DP# a parity-bit signal, they form a DATA BUS. S1-D7# is the most significant bit and has the highest priority during the ARBITRATION phase. Bit number, significance, and priority decrease downward to S1-D0#.
S1-D1#	A24	Data Bus Bit Signal 1	Data bit signal 1. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-D2#	A25	Data Bus Bit Signal 2	Data bit signal 2. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-D3#	A26	Data Bus Bit Signal 3	Data bit signal 3. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-D4#	A27	Data Bus Bit Signal 4	Data bit signal 4. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-D5#	A28	Data Bus Bit Signal 5	Data bit signal 5. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
S1-D6#	A29	Data Bus Bit Signal 6	Data bit signal 6. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-D7#	A30	Data Bus Bit Signal 7	Data bit signal 7. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
S1-DP#	A31	Data Bus Parity	Data parity bit signal. Parity is Odd. Parity is undefined during the ARBITRATION phase. See S1-D0#.
S1-I/O#	B31	Input/Output	A signal driven by a target that controls the direction of data movement on the DATA BUS with respect to an initiator. True indicates input to the initiator. This signal is also used to distinguish between SELECTION and RESELECTION phases.
S1-MSG#	B27	Message	A signal driven by a target during the MESSAGE phase.
S1-REQ#	B30	Request	A signal driven by a target to indicate a request for a REQ/ACK data transfer handshake.
S1-RST#	B26	Reset	An "OR-tied" signal that indicates the RESET condition. The RST signal may be asserted by any SCSI device at any time.
S1-SEL#	B28	Select	An "OR-tied" signal used by an initiator to select a target or by a target to reselect an initiator. NOTE: The SEL signal was not defined as "OR-tied" in SCSI-1. It has been defined as "OR-tied" in SCSI-2. This does not cause an operational problem in mixing SCSI-1 and SCSI-2 devices.

9.4.11 J901 Peripheral I/O – Video Analog (CRT–VGA) Interface

Table 35 Signals – Peripheral I/O J901 – Video Analog (CRT–VGA) Display Interface

PIN NAME	PIN# [1]	SIGNAL NAME	SIGNAL DESCRIPTION
V1-B	A6	CRT Blue	This Active High output signal is the BLUE CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm equivalent load on each pin (e.g. 75 ohm resistor on the board, in parallel with the 75 ohm CRT load).
V1-G	C4	CRT Green	This Active High output signal is the GREEN CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm equivalent load on each pin (e.g. 75 ohm resistor on the board, in parallel with the 75 ohm CRT load).
V1-HSYNC	C3	Horizontal Sync	(HSYNC or CSYNC) This Active High/Low output signal is the CRT Horizontal Sync (polarity is programmable). or the "Composite Sync" for support of various external NTSC/PAL encoder chips.
V1-R	A7	CRT Red	This Active High output signal is the RED CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm equivalent load on each pin (e.g. 75 ohm resistor on the board, in parallel with the 75 ohm CRT load).
V1-VSYNC	C2	Vertical Sync	(VSYNC or VISINT) This Active High/Low output signal is the CRT Vertical Sync (polarity is programmable) or "VSync Interval" for support of various external NTSC/PAL encoder chips.

NOTES
[1] For all of the pins in this table, the signal is gated onto corresponding pin under program control, using the 65550.ENAVEE signal (the pins are multiplexed by both the 8/16-bit panel interface and by the Video analog interface, only one of which can be active at one time, and which is controlled by 65550.ENAVEE). Full simultaneous panel and CRT operation is supported using the Video Analog interface (described in this table) for CRTs, and the 24-bit panel connector for panels.

9.4.12 J901 Peripheral I/O – Video Panel (8/16 Bit) Interface

This section applies to the compatibility panel interface, provided on J901 (96-pin DIN connector). For a description of the full 24-bit panel interface provided on J002, please refer to section 9.2 on page 64.

To use this interface, which is compatible to that for PC/II+, PC/II+i and PC/II+e Cpu boards, one of the following panel type options must be ordered:

- Monochrome SS 8-Bit Panel
- Color TFT 9/12 Bit Panel
- Color STN Extended 4-Bit Packed Panel

Additional custom interfaces will be announced when they become available.

Based on the ordered Panel Option, the PC/II+dxe board will be shipped with the appropriate straps to support the specified panel type. The purpose of the straps is to provide the correctly mapped panel data lines on the 96-pin DIN connector. Mapping occurs from the C&T 65550 controller (used on the PC/II+dxe) to the C&T 65530 controller (used on the PC/II+, PC/II+i and PC/II+e).

A table for each of the optional panel types is given below. In these tables, the signal source (from the C&T 65550 controller) is given for each panel interface pin on the 96-pin DIN connector.

Table 36 Signals – Peripheral I/O J901 – Compatible Video Panel – Mono SS 8-Bit Panels

PIN NAME	PIN# [1]	SIGNAL DESCRIPTION [3]	65550 SOURCE SIGNAL [2]
VID-P0	B2	Panel Data 0. Active High. Output.	L1-FPD8
VID-P1	B3	Panel Data 1. Active High. Output.	L1-FPD9
VID-P2	B4	Panel Data 2. Active High. Output.	L1-FPD10
VID-P3	A1	Panel Data 3. Active High. Output.	L1-FPD11
VID-P4	C5	Panel Data 4. Active High. Output.	L1-FPD12
VID-P5	A2	Panel Data 5. Active High. Output.	L1-FPD13
VID-P6	B6	Panel Data 6. Active High. Output.	L1-FPD14
VID-P7	C6	Panel Data 7. Active High. Output.	L1-FPD15
VID-P8	A3		-
VID-P9 / V1-G	C4		-
VID-P10 / V1-B	A6		-
VID-P11 / V1-R	A7		-
VID-SCK	A4	Shift Clock. This signal is the pixel clock for flat panel data. Active high. Output.	L1-SHFCLK
VID-LP / V1-HSYNC	C3	Latch Pulse. Flat Panel equivalent of HSYNC. Active high. Output.	L1-LP
VID-FRM / V1-VSYNC	C2	First Line Marker. Flat Panel equivalent of VSYNC. Active high. Output.	L1-FLM
VID-M	A5	M signal. This signal is the M-signal for panel AC drive control (may also be called ACDCLK). May also be configured as BLANK# or as Display Enable (DE) for TFT Panels. Active High. Output.	L1-M

NOTES
[1] Panel interface lines are gated onto corresponding pins under program control, using the 65550.ENAVEE signal (the pins are multiplexed by both the 8/16-bit panel interface and by the Video analog interface, only one of which can be active at one time, and which is controlled by 65550.ENAVEE). Full simultaneous panel and CRT operation is supported using the Video Analog interface (described in this table) for CRTs, and the 24-bit panel connector for panels.
[2] The source signal name corresponds to the signal name assigned on the PC/II+dxe board, a description of which is provided in the 24-bit Panel Connector (2x18) Signal Table on page 64.
[3] The Signal Description column contains a description of the Mono SS 8-Bit panel signal attached to the corresponding 96-pin DIN connector pin.
[4] Order this option using code h=0; see section 10.1 on page 99.

Table 37 Signals – Peripheral I/O J901 – Compatible Video Panel – Color TFT 9/12 Bit Panels

PIN NAME	PIN# [1]	SIGNAL DESCRIPTION [2]	65550 SOURCE SIGNAL [3]
VID-P0	B2	B0. Active High. Output.	L1-FPD1 (B1)
VID-P1	B3	B1. Active High. Output.	L1-FPD2 (B2)
VID-P2	B4	B2. Active High. Output.	L1-FPD3 (B3)
VID-P3	A1	B3. Active High. Output.	L1-FPD4 (B4)
VID-P4	C5	G0. Active High. Output.	L1-FPD7 (G2)
VID-P5	A2	G1. Active High. Output.	L1-FPD8 (G3)
VID-P6	B6	G2. Active High. Output.	L1-FPD9 (G4)
VID-P7	C6	G3. Active High. Output.	L1-FPD10 (G5)
VID-P8	A3	R0. Active High. Output.	L1-FPD12 (R1)
VID-P9 / V1-G	C4	R1. Active High. Output.	L1-FPD13 (R2)
VID-P10 / V1-B	A6	R2. Active High. Output.	L1-FPD14 (R3)
VID-P11 / V1-R	A7	R3. Active High. Output.	L1-FPD15 (R4)
VID-SCK	A4	Shift Clock. This signal is the pixel clock for flat panel data. Active high. Output.	L1-SHFCLK
VID-LP / V1-HSYNC	C3	Latch Pulse. Flat Panel equivalent of HSYNC. Active high. Output.	L1-LP
VID-FRM / V1-VSYNC	C2	First Line Marker. Flat Panel equivalent of VSYNC. Active high. Output.	L1-FLM
VID-M	A5	M signal. This signal is the M-signal for panel AC drive control (may also be called ACDCLK). May also be configured as BLANK# or as Display Enable (DE) for TFT Panels. Active High. Output.	L1-M

NOTES
[1] Panel interface lines are gated onto corresponding pins under program control, using the 65550.ENAVEE signal (the pins are multiplexed by both the 8/16-bit panel interface and by the Video analog interface, only one of which can be active at one time, and which is controlled by 65550.ENAVEE). Full simultaneous panel and CRT operation is supported using the Video Analog interface (described in this table) for CRTs, and the 24-bit panel connector for panels.
[2] The Signal Description column contains a description of the Color TFT 9/12 Bit signal attached to the corresponding 96-pin DIN connector pin.
[3] The 65550 Source Signal name corresponds to the signal name assigned on the PC/II+dxe board, a description of which is provided in the 24-bit Panel Connector (2x18) Signal Table on page 64.
[4] Order this option using code h=1; see section 10.1 on page 99.

Table 38 Signals – Peripheral I/O J901 – Compatible Video Panel – Color STN Ext 4-Bit Pack Panels

PIN NAME	PIN# [1]	SIGNAL DESCRIPTION [3]	65550 SOURCE SIGNAL [2]
VID-P0	B2	R1 - G1. Active High. Output. In extended 4-bit pack mode, pixel values Rn-Gn-Bn are shifted into a 16-bit register every SHFCLKU period. The 8 even bits are output on P0 through P7 on the falling edge of SHFCLKU; then the 8 odd bits are output on P0 through P7 on the rising edge of SHFCLKU (the falling edge of SHFCLKL). The resulting sequence, in P0-P7 order, is R1-B1-G2-R3-B3-G4-R5-B5 G1-R2-B2-G3-R4-B4-G5-R6 For the next clock period, the next 16 bits of Rn-Gn-Bn values are shifted into the 16-bit register and output using the same packing algorithm.	L1-FPD0
VID-P1	B3	B1 - R2. Active High. Output.	L1-FPD1
VID-P2	B4	G2 - B2. Active High. Output.	L1-FPD2
VID-P3	A1	R3 - G3. Active High. Output.	L1-FPD3
VID-P4	C5	B3 - R4. Active High. Output.	L1-FPD4
VID-P5	A2	G4 - B4. Active High. Output.	L1-FPD5
VID-P6	B6	R5 - G5. Active High. Output.	L1-FPD6
VID-P7	C6	B5 - R6. Active High. Output.	L1-FPD7
VID-P8	A3		SHFCLKU
VID-P9 / V1-G	C4		-
VID-P10 / V1-B	A6		-
VID-P11 / V1-R	A7		-
VID-SCK	A4	Shift Clock. This signal is the pixel clock for flat panel data. Active high. Output.	L1-SHFCLK
VID-LP / V1-HSYNC	C3	Latch Pulse. Flat Panel equivalent of HSYNC. Active high. Output.	L1-LP
VID-FRM / V1-VSYNC	C2	First Line Marker. Flat Panel equivalent of VSYNC. Active high. Output.	L1-FLM
VID-M	A5	M signal. This signal is the M-signal for panel AC drive control (may also be called ACDCLK). May also be configured as BLANK# or as Display Enable (DE) for TFT Panels. Active High. Output.	L1-M

NOTES

[1] Panel interface lines are gated onto corresponding pins under program control, using the 65550.ENAVEE signal (the pins are multiplexed by both the 8/16-bit panel interface and by the Video analog interface, only one of which can be active at one time, and which is controlled by 65550.ENAVEE). Full simultaneous panel and CRT operation is supported using the Video Analog interface (described in this table) for CRTs, and the 24-bit panel connector for panels.

[2] The source signal name corresponds to the signal name assigned on the PC/II+dxe board, a description of which is provided in the 24-bit Panel Connector (2x18) Signal Table on page 64.

[3] The Signal Description column contains a description of the Color Extended 4-Bit Pack panel signal attached to the corresponding 96-pin DIN connector pin.

[4] Order this option using code h=2; see section 10.1 on page 99.

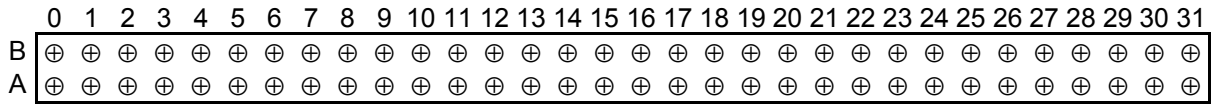
9.5 J902 – ISA Bus Connector – 8 Bit

This section describes the 8-bit ISA Bus connector; please refer to section 9.8 for a description of the 16-bit (I/O) bus extension.

The 64-pin (2x32) 8-bit ISA Bus connector (J902) is an option on the PC/II+dxe board.

For ISA bus signals, AC Bus termination provides termination close to the characteristic impedance of the signal line without exceeding the DC output current capabilities of the drivers. This increases data integrity and system reliability. A resistor-capacitor network of 40-60 ohms in series with 30-70 pF can be connected between each bus signal and ground. All 8-bit ISA Bus signals can be driven with devices capable of providing 4 mA sink current. Please refer to the PC ISA Bus Specification document for additional information on the ISA bus.

Figure 6 Diagram – ISA 8-bit Bus J902 – 2 X 32 .100" Header



NOTES

[1] Top (component) view is shown.

[2] The last 31 columns (A1 through A31, and B1 through B31) of this header correspond to the PC Bus interface.

[3] Warning – the following pins used on the PC/II+dxe 8-bit ISA bus header do not correspond to those of the XT/AT ISA bus interface, in particular they are NOT power pins. Do NOT apply power to these pins. They are: J902.B5 (-5V) is now IRQ15 or IRQ10; J902.B7 (-12V) is now DACK16#; and J902.B9 (+12V) is now IRQ14 or DRQ16.

Table 39 Pinout – ISA 8-bit Bus J902 (Rows A and B) – 2 X 32 .100" Header

POS [1,2]	ROW A	ROW B
0	GND	+5V
1	IOCHK#	GND
2	SD7	RESETDRV#
3	SD6	+5V
4	SD5	IRQ2
5	SD4	IRQ15 OR IRQ10 [3]
6	SD3	DRQ2
7	SD2	DACK16# [4]
8	SD1	NOWS#
9	SD0	IRQ14 OR DRQ16 [5]
10	IORDY	GND
11	AEN	MEMW#
12	SA19	MEMR#
13	SA18	IOW#
14	SA17	IOR#
15	SA16	DACK3#
16	SA15	DRQ3
17	SA14	DACK1#
18	SA13	DRQ1
19	SA12	REFRESH#
20	SA11	BCLK
21	SA10	IRQ7
22	SA9	IRQ6
23	SA8	IRQ5
24	SA7	IRQ4
25	SA6	IRQ3
26	SA5	DACK2#
27	SA4	TC
28	SA3	BALE
29	SA2	+5V
30	SA1	OSC
31	SA0	GND

NOTES
[1] Refer to the XT/AT ISA Bus Specification.
[2] Pin numbering (A1-A31 and B1-B31) complies with the XT/AT ISA 8-bit Bus Specification.
[3] Pin B5 was -5V, but has been reassigned to IRQ15 or IRQ10; do NOT apply power to this pin.
[4] Pin B7 was -12V, but has been reassigned to DACK16#; do NOT apply power to this pin.
[5] Pin B9 was +12V but has been reassigned to IRQ14 or DRQ16; do NOT apply power to this pin.

Table 40 Signals – J902 – ISA 8-bit Bus

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
DACK16#	B7	DACK16#	DMA Acknowledge 6 & 7. Active Low Output. This signal is generated by the logical AND of the on-board DACK6# and DACK7# signals. DMA Acknowledge 6. In general, this signal is raised by the DMA controller (after the DMA controller receives control of the bus from the Cpu) in response to a corresponding DMA Request signal that was asserted by a peripheral wishing to perform a DMA transfer. DMA Acknowledge 7. In general, this signal is raised by the DMA controller (after the DMA controller receives control of the bus from the Cpu) in response to a corresponding DMA Request signal that was asserted by a peripheral wishing to perform a DMA transfer. Note – on a standard ISA bus, this pin is -12V. On the PC/II+dxe ISA bus, this is NOT a power pin.
DRQ16#	B9	IRQ14 OR DRQ6 OR DRQ7	MA Request 6 or 7, or Interrupt Request 14. Active high input. This input signal is wire or'ed into IRQ14, DRQ6 and DRQ7, one of which can be unmasked, one at a time, by a program or bios to allow this input signal to function in its capacity. Interrupt Request Level 14. Active high input, Asynchronous. Signals an interrupt request on a low-to-high transition (if the interrupt controller level 14 has been programmed into edge-triggered mode), or when it is at a high level (if the interrupt controller level 14 has been programmed into level-triggered mode). Remains high until acknowledged (in level-triggered mode). Priorities are (highest) 0-1, 8-15, 3-7. DMA Request 6. Active high input, Asynchronous. Driven high by a peripheral to initiate DMA transfer (after the DMA controller has been appropriately programmed for a transfer), and returned to low by peripheral after DACK6# has been asserted by the DMA controller. DMA Request 7. Active high input, Asynchronous. Driven high by a peripheral to initiate DMA transfer (after the DMA controller has been appropriately programmed for a transfer), and returned to low by peripheral after DACK7# has been asserted by the DMA controller. Note – on a standard ISA bus, this pin is +12V. On the PC/II+dxe ISA bus, this is NOT a power pin.

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
IRQ15 OR IRQ10	B5	IRQ15 OR IRQ10	Interrupt Request Level 15 or 10. Active high input, Asynchronous. Signals an interrupt request on a low-to-high transition (if the interrupt controller level 15 or 10 has been programmed into edge-triggered mode), or when it is at a high level (if the interrupt controller level 15 or 10 has been programmed into level-triggered mode). Remains high until acknowledged (in level-triggered mode). Priorities are (highest) 0-1, 8-15, 3-7. Note – on a standard ISA bus, this pin is -5V. On the PC/II+dxe ISA bus, this is NOT a power pin.
ISA_+5V_1	B0	+5V	+5V
ISA_+5V_2	B3	+5V	+5V
ISA_+5V_3	B29	+5V	+5V
ISA_AEN	A11	AEN	Address Enable. Active high output. This signal is bus hold acknowledge. When asserted, I/O devices ignore the address & I/O command lines, which allows a DMA controller to proceed with a DMA transfer.
ISA_BALE	B28	BALE	Buffered Address Latch Enable. The SA address bus is valid from the falling edge of BALE to the end of the bus cycle, while the LA address bus must be latched on the falling edge of BALE.
ISA_BCLK	B20	BCLK	Bus Clock. Reference for all bus signals. This signal may vary in frequency. It can be configured in the BIOS to operate at differing frequencies, depending upon special timing requirements of attached peripherals. It is configured by default to operate at 8.00 MHz.
ISA_DACK1#	B17	DACK1#	DMA Acknowledge 1. Active Low Output. In general, this signal is raised by the DMA controller (after the DMA controller receives control of the bus from the Cpu) in response to a corresponding DMA Request signal that was asserted by a peripheral wishing to perform a DMA transfer.
ISA_DACK2#	B26	DACK2#	DMA Acknowledge 2. Active Low Output. In general, this signal is raised by the DMA controller (after the DMA controller receives control of the bus from the Cpu) in response to a corresponding DMA Request signal that was asserted by a peripheral wishing to perform a DMA transfer.
ISA_DACK3#	B15	DACK3#	DMA Acknowledge 3. Active Low Output. In general, this signal is raised by the DMA controller (after the DMA controller receives control of the bus from the Cpu) in response to a corresponding DMA Request signal that was asserted by a peripheral wishing to perform a DMA transfer.

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
ISA_DRQ1	B18	DRQ1	DMA Request 1. Active high input, Asynchronous. Driven high by a peripheral to initiate DMA transfer (after the DMA controller has been appropriately programmed for a transfer), and returned to low by peripheral after DACK1# has been asserted by the DMA controller.
ISA_DRQ2	B6	DRQ2	DMA Request 2. Active high input, Asynchronous. Driven high by a peripheral to initiate DMA transfer (after the DMA controller has been appropriately programmed for a transfer), and returned to low by peripheral after DACK2# has been asserted by the DMA controller.
ISA_DRQ3	B16	DRQ3	DMA Request 3. Active high input, Asynchronous. Driven high by a peripheral to initiate DMA transfer (after the DMA controller has been appropriately programmed for a transfer), and returned to low by peripheral after DACK3# has been asserted by the DMA controller.
ISA_GND1	A0	GND	Ground – 0V
ISA_GND2	B1	GND	Ground – 0V
ISA_GND3	B10	GND	Ground – 0V
ISA_GND4	B31	GND	Ground – 0V
ISA_IOCHK#	A1	IOCHK#	I/O (channel) error check condition. Active low input. When active, a non-maskable interrupt (NMI) is generated by the 2089 and signaled to the Cpu. I/O port 0x70 bit 7 must be set to 0 to enable NMI interrupts from the 2089 to the Cpu. IOCHK must also be enabled (port 0x61)
ISA_IOR#	B14	IOR#	I/O Read Command. Active low output. Asserted by the 2089 in an I/I bus cycle, to instruct the peripheral to drive its data onto the data bus.
ISA_IORDY	A10	IORDY	I/O (channel) Ready. Active high input. When held low by a peripheral, the peripheral is preventing the bus cycle from ending. The peripheral raises this line again at the end of its bus cycle. The peripheral can therefore cause its memory or I/O cycle to be increased in length, allowing more time for it to complete the transfer. This signal should not be held low for more than 2.5 microseconds.
ISA_IOW#	B13	IOW#	I/O Write Command. Active low output. Asserted by the 2089 in an I/O bus cycle, to instruct the peripheral to latch the contents of the incoming data bus.

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
ISA_IRQ2	B4	IRQ2	Interrupt Request Level 2. Active high input, Asynchronous. Signals an interrupt request on a low-to-high transition (if the interrupt controller level 2 has been programmed into edge-triggered mode), or when it is at a high level (if the interrupt controller level 2 has been programmed into level-triggered mode). Remains high until acknowledged (in level-triggered mode). Priorities are (highest) 0-1, 8-15, 3-7.
ISA_IRQ3	B25	IRQ3	Interrupt Request Level 3. Active high input, Asynchronous. Signals an interrupt request on a low-to-high transition (if the interrupt controller level 3 has been programmed into edge-triggered mode), or when it is at a high level (if the interrupt controller level 3 has been programmed into level-triggered mode). Remains high until acknowledged (in level-triggered mode). Priorities are (highest) 0-1, 8-15, 3-7.
ISA_IRQ4	B24	IRQ4	Interrupt Request Level 4. Active high input, Asynchronous. Signals an interrupt request on a low-to-high transition (if the interrupt controller level 4 has been programmed into edge-triggered mode), or when it is at a high level (if the interrupt controller level 4 has been programmed into level-triggered mode). Remains high until acknowledged (in level-triggered mode). Priorities are (highest) 0-1, 8-15, 3-7.
ISA_IRQ5	B23	IRQ5	Interrupt Request Level 5. Active high input, Asynchronous. Signals an interrupt request on a low-to-high transition (if the interrupt controller level 5 has been programmed into edge-triggered mode), or when it is at a high level (if the interrupt controller level 5 has been programmed into level-triggered mode). Remains high until acknowledged (in level-triggered mode). Priorities are (highest) 0-1, 8-15, 3-7.
ISA_IRQ6	B22	IRQ6	Interrupt Request Level 6. Active high input, Asynchronous. Signals an interrupt request on a low-to-high transition (if the interrupt controller level 6 has been programmed into edge-triggered mode), or when it is at a high level (if the interrupt controller level 6 has been programmed into level-triggered mode). Remains high until acknowledged (in level-triggered mode). Priorities are (highest) 0-1, 8-15, 3-7.
ISA_IRQ7	B21	IRQ7	Interrupt Request Level 7. Active high input, Asynchronous. Signals an interrupt request on a low-to-high transition (if the interrupt controller level 7 has been programmed into edge-triggered mode), or when it is at a high level (if the interrupt controller level 7 has been programmed into level-triggered mode). Remains high until acknowledged (in level-triggered mode). Priorities are (highest) 0-1, 8-15, 3-7.

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
ISA_NOWS#	B8	NOWS#	Zero Wait State. Active low input. Asserted by a peripheral that wishes to complete a memory or I/O cycle without inserted wait states. If the processor is generating wait states, then assertion of NOWS will cause no further wait states to be generated. Typically, assertion of this signal causes the memory or I/O cycle to be decreased in length.
ISA_OSC	B30	OSC	14.318 MHz, 50% duty cycle. Not synchronized to the system clock.
ISA_REFRESH#	B19	REFRESH#	Refresh. Active low input/output. Asserted by the memory refresh controller, acting as bus master, to indicate that a refresh cycle is in progress.
ISA_RESETDRV#	B2	RESETDRV#	Reset Drive. Active high output. Asserted during a system reset condition (and at power up). Synchronized to falling edge of CLK.
ISA_SA0	A31	SA0	System Address Bit 0. Bidirectional, tri-state.
ISA_SA1	A30	SA1	System Address Bit 1. Bidirectional, tri-state.
ISA_SA2	A29	SA2	System Address Bit 2. Bidirectional, tri-state.
ISA_SA3	A28	SA3	System Address Bit 3. Bidirectional, tri-state.
ISA_SA4	A27	SA4	System Address Bit 4. Bidirectional, tri-state.
ISA_SA5	A26	SA5	System Address Bit 5. Bidirectional, tri-state.
ISA_SA6	A25	SA6	System Address Bit 6. Bidirectional, tri-state.
ISA_SA7	A24	SA7	System Address Bit 7. Bidirectional, tri-state.
ISA_SA8	A23	SA8	System Address Bit 8. Bidirectional, tri-state.
ISA_SA9	A22	SA9	System Address Bit 9. Bidirectional, tri-state.
ISA_SA10	A21	SA10	System Address Bit 10. Bidirectional, tri-state.
ISA_SA11	A20	SA11	System Address Bit 11. Bidirectional, tri-state.
ISA_SA12	A19	SA12	System Address Bit 12. Bidirectional, tri-state.
ISA_SA13	A18	SA13	System Address Bit 13. Bidirectional, tri-state.
ISA_SA14	A17	SA14	System Address Bit 14. Bidirectional, tri-state.
ISA_SA15	A16	SA15	System Address Bit 15. Bidirectional, tri-state.
ISA_SA16	A15	SA16	System Address Bit 16. Bidirectional, tri-state.
ISA_SA17	A14	SA17	System Address Bit 17. Bidirectional, tri-state.
ISA_SA18	A13	SA18	System Address Bit 18. Bidirectional, tri-state.
ISA_SA19	A12	SA19	System Address Bit 19. Bidirectional, tri-state.
ISA_SD0	A9	SD0	System data bit 0. Active high bi-directional, tri-stated.
ISA_SD1	A8	SD1	System data bit 1. Active high bi-directional, tri-stated.
ISA_SD2	A7	SD2	System data bit 2. Active high bi-directional, tri-stated.
ISA_SD3	A6	SD3	System data bit 3. Active high bi-directional, tri-stated.
ISA_SD4	A5	SD4	System data bit 4. Active high bi-directional, tri-stated.
ISA_SD5	A4	SD5	System data bit 5. Active high bi-directional, tri-stated.

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
ISA_SD6	A3	SD6	System data bit 6. Active high bi-directional, tri-stated.
ISA_SD7	A2	SD7	System data bit 7. Active high bi-directional, tri-stated.
ISA_SMEMR#	B12	SMEMR#	ISA bus Memory Write Command. Active low output. Asserted if current bus cycle is an ISA memory read cycle that targets memory within the first 1MB of physical memory space. This signal is tri-stated when memory is addressed outside the first 1MB of physical memory space. Note – this signal is derived within the 2089 from MEMR#. Please refer to the 2089 datasheet for more information.
ISA_SMEMW#	B11	SMEMW#	ISA bus Memory Read Command. Active low output. Asserted if current bus cycle is an ISA memory write cycle that targets memory within the first 1MB of physical memory space. This signal is tri-stated when memory is addressed outside the first 1MB of physical memory space. Note – this signal is derived within the 2089 from MEMW#. Please refer to the 2089 datasheet for more information.
ISA_TC	B27	TC	Terminal Count. Active high output. The DMA controller in the 2089 pulses this line to indicate that the terminal count (the counter) in any DMA channel is reached, and the DMA transfer is complete.

NOTES
[1] *Refer to the XT/AT ISA Bus Specification.*
[2] *Pin numbering (A1-A31 and B1-B31) complies with the XT/AT ISA 8-bit Bus Specification.*
[3] *Pin B5 was -5V, but has been reassigned to IRQ15 or IRQ10; do NOT apply power to this pin.*
[4] *Pin B7 was -12V, but has been reassigned to DACK16#; do NOT apply power to this pin.*
[5] *Pin B9 was +12V but has been reassigned to IRQ14 or DRQ16; do NOT apply power to this pin.*

9.6 J903 – Ethernet Connector (2x5 .100 Inch Header)

Figure 7 Diagram – Ethernet J903 – 2x5 Pin .100 Inch R/A Male Header

NOTES
[1] Top (component) view is shown.

Table 41 Pinout – Ethernet J903 – 2x5 Pin .100 Inch R/A Male Header

PIN GROUP	PIN#	PIN NAME
E2-ETHERNET2 AUI	1	E2-CLSN-
E2-ETHERNET2 AUI	2	E2-CLSN+
E1-ETHERNET1 10BASE-T	3	E1-RD-
E1-ETHERNET1 10BASE-T	4	E1-RD+
E2-ETHERNET2 AUI	5	E2-RCV-
E2-ETHERNET2 AUI	6	E2-RCV+
E1-ETHERNET1 10BASE-T	7	E1-TD-
E1-ETHERNET1 10BASE-T	8	E1-TD+
E2-ETHERNET2 AUI	9	E2-TRMT-
E2-ETHERNET2 AUI	10	E2-TRMT+

Table 42 Signals – Ethernet J903 – 10Base-T Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
E1-TD-	7	Negative Transmit Data	Negative Differential Manchester-encoded Transmit Data Line, 10 Mbps, from onboard 10 BASE T Isolation Transformer (1:SQRT(2)) Pin 11. Connect to external RJ45 connector Pin 2.
E1-TD+	8	Positive Transmit Data	Positive Differential Manchester-encoded Transmit Data Line, 10 Mbps, from onboard 10 BASE T Isolation Transformer (1:SQRT(2)) Pin 9. Connect to external RJ45 connector Pin 1.
E1-RD-	3	Negative Receive Data	Negative Differential Manchester-encoded Receive Data Line, 10 Mbps, to onboard 10 BASE T Isolation Transformer (1:1) Pin 16. Connect to external RJ45 connector Pin 6.
E1-RD+	4	Positive Receive Data	Positive Differential Manchester-encoded Receive Data Line, 10 Mbps, to onboard 10 BASE T Isolation Transformer (1:1) Pin 14. Connect to external RJ45 connector Pin 3.

Table 43 Signals – Ethernet J903 – AUI Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
E2-CLSN-	1	Negative Collision In	Negative Differential AUI Collision Input Line, to onboard AUI Isolation Transformer Pin 13. Connect to external DB15 connector Pin 9.
E2-CLSN+	2	Positive Collision In	Positive Differential AUI Collision Input Line, to onboard AUI Isolation Transformer Pin 10. Connect to external DB15 connector Pin 2.
E2-TRMT-	9	Negative Transmit Data	Negative Differential Manchester-encoded Transmit Data Line, 10 Mbps, from onboard AUI Isolation Transformer Pin 16. Connect to external DB15 connector Pin 10.
E2-TRMT+	10	Positive Transmit Data	Positive Differential Manchester-encoded Transmit Data Line, 10 Mbps, from onboard AUI Isolation Transformer Pin 15. Connect to external DB15 connector Pin 3.
E2-RCV-	5	Negative Receive Data	Negative Differential Manchester-encoded Receive Data Line, 10 Mbps, to onboard AUI Isolation Transformer (1:1) Pin 10. Connect to external DB15 connector Pin 12.
E2-RCV+	6	Positive Receive Data	Positive Differential Manchester-encoded Receive Data Line, 10 Mbps, to onboard AUI Isolation Transformer (1:1) Pin 9. Connect to external DB15 connector Pin 5.

9.7 J904 – IDE Connector (2x22 2mm Header)

Table 44 Pinout & Signals – IDE/ATA Interface J904 – 44 pin 2mm pitch

PIN NAME	PIN #	SIGNAL NAME	SIGNAL DESCRIPTION
PWRGOOD	1	Power Good	Power Good Indicator. Active high output. This signal is pulled low by the Cpu board to signal the peripheral that power has failed or a reset condition has occurred. The Cpu board pulls this signal low when one of the following conditions occurs: (a) an on-board voltage regulator is unable to maintain its output voltage (due possibly to a power failure for example), (b) the Reset Switch signal is asserted, or (c) the Watchdog is enabled and a watchdog event occurs. This signal remains low until all of these conditions return to their normal state.
GND	2	Ground	Ground
A1-DD7	3	Data Bus 7	IDE Channel Data Bit 7.
A1-DD8	4	Data Bus 8	IDE Channel Data Bit 8.
A1-DD6	5	Data Bus 6	IDE Channel Data Bit 6.
A1-DD9	6	Data Bus 9	IDE Channel Data Bit 9.
A1-DD5	7	Data Bus 5	IDE Channel Data Bit 5.
A1-DD10	8	Data Bus 10	IDE Channel Data Bit 10.
A1-DD4	9	Data Bus 4	IDE Channel Data Bit 4.
A1-DD11	10	Data Bus 11	IDE Channel Data Bit 11.
A1-DD3	11	Data Bus 3	IDE Channel Data Bit 3.
A1-DD12	12	Data Bus 12	IDE Channel Data Bit 12.
A1-DD2	13	Data Bus 2	IDE Channel Data Bit 2.
A1-DD13	14	Data Bus 13	IDE Channel Data Bit 13.
A1-DD1	15	Data Bus 1	IDE Channel Data Bit 1.
A1-DD14	16	Data Bus 14	IDE Channel Data Bit 14.
A1-DD0	17	Data Bus 0	IDE Channel Data Bit 0.
A1-DD15	18	Data Bus 15	IDE Channel Data Bit 15.
GND	19	Ground	Ground
N/C	20	N/C	Not connected
N/C	21	N/C	Not connected
GND	22	Ground	Ground
A1-DIOW#	23	IO Write Command	This signal is the IOW command output pin to notify the IDE device that the available Write Data is already asserted by the onboard IDE controller.
GND	24	Ground	Ground
A1-DIOR#	25	IO Read Command	This signal is the IOR command output pin to notify the IDE device to assert the Read Data.

PIN NAME	PIN #	SIGNAL NAME	SIGNAL DESCRIPTION
GND	26	Ground	Ground
A1-IORDY	27	IDE Ready	This is the input pin from the IDE Channel to indicate the IDE device is ready to terminate the IDE command. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready.
CSEL	28	Cable Select	Cable Select allows each device to determine whether it should configure itself as device 0 or device 1. On IDE buses which require this selection to be done using the cable select method, then this pin should be at GROUND potential, and in this case, the IDE connector (J904) should have it's CSEL grounding resistor installed at manufacturing time. If the Cable Select method is not to be used (for example, drives self-configure using inter-drive communication), then this pin is typically a NO CONNECT. Please specify the Cable Select option at order time.
N/C	29	N/C	Not connected
GND	30	Ground	Ground
A1-INTRQ	31	IDE Interrupt	This is the input pin from the IDE Channel to signal an interrupt. It will be routed to the appropriate Int14 8259 interrupt controller input.
A1-IOCS16#	32	Device 16-Bit I-O	This is the input pin from the IDE device which, during PIO transfer modes 0, 1 or 2, indicates to the host system that the 16-bit data port has been addressed and that the device is prepared to send or receive a 16-bit data word.
A1-DA1	33	Address Bus 1	This signal is Address Bit 1 of the ATA Address Bus that is connected to IDE Channel.
QT_PDIAG-	34	Passed Diagnostics	This signal is asserted by Device 1 to indicate to Device 0 that it has completed diagnostics. Tie to Pin 34 of additional drive connectors for multiple drive configurations; This pin is NOT tied to the host IDE controller, rather it is used only for inter-drive communication (i.e. this pin is a N/C on the Cpu board).
A1-DA0	35	Address Bus 0	This signal is Address Bit 0 of the ATA Address Bus that is connected to IDE Channel.
A1-DA2	36	Address Bus 2	This signal is Address Bit 2 of the ATA Address Bus that is connected to IDE Channel.
A1-CS0#	37	Chip Select 1 for Ch 0	This is the Chip Select 1 command output pin to enable the IDE device to watch the Read/Write Command.
A1-CS1#	38	Chip Select 3 for Ch 1	This is the Chip Select 3 command output pin to enable the IDE device to watch the Read/Write Command.
QT_DASP-	39	Device Active, or Slave (Device 1) Present	This is a time-multiplexed signal that indicates that a device is active, or that Device 1 is present. Tie this pin to Pin 39 of additional drive connectors for multiple drive configurations. This pin is NOT tied to the host IDE controller (i.e. it is a N/C on the Cpu board), rather it is used only for inter-drive communication.
GND	40	Ground	Ground

PIN NAME	PIN #	SIGNAL NAME	SIGNAL DESCRIPTION
+5V	41	+5V	POWER +5V
+5V	42	+5V	POWER +5V
GND	43	Ground	Ground
GND	44	Ground	Ground

9.8 J905 – ISA Bus Extension Connector – 16-Bit (I/O)

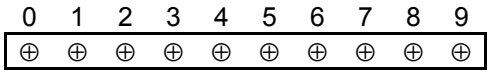
This section describes the 16-bit (I/O) ISA Bus extension connector; please refer to section 9.5 for a description of the 8-bit ISA bus connector.

The 10-pin (1x10) 16-bit (I/O) ISA Bus connector (J905) is an option on the PC/II+dxe board.

For ISA bus signals, AC Bus termination provides termination close to the characteristic impedance of the signal line without exceeding the DC output current capabilities of the drivers. This increases data integrity and system reliability. A resistor-capacitor network of 40 to 60 ohms in series with 30 to 70 pF can be connected between each bus signal and ground. All 16-bit ISA Bus signals (except for BS16#) can be driven with devices capable of providing 4 mA sink current. The BS16# signal can be driven with devices capable of providing 10 mA sink current.

Please refer to the PC ISA Bus Specification document for additional information on the ISA bus.

Figure 8 Diagram – ISA 16-bit (I/O) Bus Extension J905 – 1 x 10 .100" Header



NOTES
[1] Top (component) view is shown.

Table 45 Pinout – ISA 16-bit (I/O) Bus Extension J905 – 1 X 10 .100" Header

PIN [1,2]	PIN NAME
1	BS16# [3]
2	SD15
3	SD14
4	SD13
5	SD12
6	SD11
7	SD10
8	SD9
9	SD8
10	SBHE#

NOTES
[1] Refer to the AT ISA Bus Specification. The signals in the 16-bit bus extension are present ONLY in the AT bus specification; they were not part of the XT bus specification, which is an 8-bit bus.
[2] Pin numbering (1-10) is unique to PC/II+dxe; pins J905-9 to J905-2 (SD8-SD15) correspond to AT bus pins C11-C18; pin J905-10 (SBHE#) corresponds to AT bus pin C1
[3] BS16# is an active-low input signal from a peripheral, when driven low the peripheral is requesting a 16-bit I/O cycle; this line has a pull-up resistor, therefore the default I/O cycle when this signal is not driven is 8-bit.

Table 46 Signals – J905 – ISA 16-bit (I/O) Bus

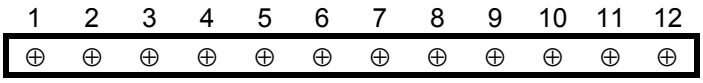
PIN NAME [1]	PIN# [2]	SIGNAL NAME	SIGNAL DESCRIPTION
BS16# [3]	1	BS16#	Bus Select 16. Active low input. This signal is driven low by a peripheral that wishes to execute a 16-bit I/O cycle. When inactive, an 8-bit bus cycle is requested. The BS16# signal is equivalent to the IOCS16# and the MEMCS16# signal. I/O cycles with BS16# inactive (16-bit bus) must be qualified with IOR# and IOW#, or with the top bits (A15 to A19) addressing 00000hex.
ISA_SBHE#	10	SBHE#	System Bus High Byte Enable. Active low tri-state. This signal indicates that SD[8:15] carries a valid data byte for the current bus cycle.
ISA_SD8	9	SD8	System data bit 8. Active high bi-directional, tri-stated.
ISA_SD9	8	SD9	System data bit 9. Active high bi-directional, tri-stated.
ISA_SD10	7	SD10	System data bit 10. Active high bi-directional tri-stated.
ISA_SD11	6	SD11	System data bit 11. Active high bi-directional tri-stated.
ISA_SD12	5	SD12	System data bit 12. Active high bi-directional tri-stated.
ISA_SD13	4	SD13	System data bit 13. Active high bi-directional tri-stated.
ISA_SD14	3	SD14	System data bit 14. Active high bi-directional tri-stated.
ISA_SD15	2	SD15	System data bit 15. Active high bi-directional tri-stated.

NOTES
[1] Refer to the AT ISA Bus Specification. The signals in the 16-bit bus extension are present ONLY in the AT bus specification; they were not part of the XT bus specification, which is an 8-bit bus.
[2] Pin numbering (1-10) is unique to PC/II+dxe; pins J905-9 to J905-2 (SD8-SD15) correspond to AT bus pins C11-C18; pin J905-10 (SBHE#) corresponds to AT bus pin C1
[3] BS16# is an active-low input signal from a peripheral, when driven low the peripheral is requesting a 16-bit I/O cycle; this line has a pull-up resistor, therefore the default I/O cycle when this signal is not driven is 8-bit.

9.9 J906 – Alternate +5V Power Connector – 1x12 Pin Header

The PC/II+dxe is normally supplied with a single +5V source of power, that is passed to the board using connector J901 (the 96-pin DIN connector). The board may alternatively (or simultaneously) be supplied with +5V using this header (J906). If both J901 (the 96-pin DIN connector) and J906 are simultaneously used to supply power to PC/II+dxe, both must be sourced from a single supply.

Figure 9 Diagram – Alternate +5v Power Header J906 – 1x12 PIN .100" R/A Male Header



NOTES
[1] Top (component) view is shown.

Table 47 Pinout – Alternate +5v Power J906 – 1x12 PIN .100" R/A Male Header

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
+5V	1	+5V	+5v
+5V	2	+5V	+5v
+5V	3	+5V	+5v
GND/KEY	4	GND/KEY	Ground (or Key)
GND	5	GND	Ground
GND	6	GND	Ground
GND	7	GND	Ground
GND	8	GND	Ground
GND	9	GND	Ground
+5V	10	+5V	+5v
+5V	11	+5V	+5v
+5V	12	+5V	+5v

9.10 JP05 – Mouse Connector – 1x2 Pin Header

Table 48 Signals – JP05 – Mouse Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
M1-CLK	2	Mouse Clock	This output is the PS2 Mouse clock.
M1-DAT	1	Mouse Data	This input is the mouse serial data line.

10 Ordering Information

The PC/II+dxe may be ordered directly from Megatel or through one of our representatives. Inquire today! Small quantity orders (1-4) are normally available within 2 weeks. For larger orders, please allow 4 to 6 weeks for delivery.

10.1 PC/II+dxe Product Numbering

To determine the model number for a specifically configured PC/II+dxe board, use the guide below. Please contact your agent, distributor or megatel if you need assistance. There are a large number of options, and we have an easy-to-use model number calculator on our Website http://www.megatel.ca to help you.

Generic PC/II+dxe Product Number :

	Connector System	Processor	Memory	-	Video	Ethernet	Flash Array	Flash Disk-on-Chip Socket	SCSI	Real-Time Clock & Battery	Serial I/O	-	Cache Memory Bus Protocol	SCSI Assignment	Watchdog	IDE Cable Select	ISA IRQ10 Mapping	ISA DACK16# Mapping	ISA IRQ14 Mapping	Compatible 8/16-Bit Panel Type	8/16-bit Panel P8 Mapping	8/16-bit Panel M-Signal Mapping	ENAVEE Polarity		IDE Header	CPU Fan 5V Connector	Mouse Header	Full 24-Bit Panel Connector	Power Supply Arrangement
PC/II+DXE/	L	P	M	-	V	E	F	H	J	K	S	-	a	b	c	d	e	f	g	h	j	k	n	-	t	u	v	w	r

Replace each letter following '/' by the code value given in tables below. '-'s are optional, and ‘0’s are required. Specify the full model number.

Options available (given below) are described in the following pages.

Option L – 96-pin I/O & ISA Connector System
Option P – Processor
Option M – Memory
Option V – Video
Option E – Ethernet
Option F – Flash Array
Option H – Flash Disk-on-Chip Socket
Option J – SCSI
Option K – Real-Time Clock & Battery
Option S – Serial
Option a – Cache Memory Bus Protocol
Option b – SCSI Assignment
Option c – Watchdog
Option d – IDE Cable Select
Option e – ISA IRQ10 Mapping
Option f – ISA DACK16# Mapping
Option g – ISA IRQ14 Mapping
Option h – Compatible 8/16-bit Panel Type
Option j – 8/16-bit Panel P8 Mapping
Option k – 8/16-bit Panel M-signal Mapping
Option n – ENAVEE Polarity
Option t – IDE Header
Option u – Cpu Fan (5v) Connector
Option v – Mouse Header
Option w – Full 24-bit Panel Connector
Option r – Power Supply Arrangement

10.2 PC/II+dxe Specific Order Example

Example :

	Connector System	Processor	Memory		Video	Ethernet	Flash Array	Flash Disk-on-Chip Socket	SCSI	Real-Time Clock & Battery	Serial I/O		Cache Memory (L1) Bus Protocol	SCSI Assignment	Watchdog	IDE Cable Select	ISA IRQ10 Mapping	ISA DACK16# Mapping	ISA IRQ14 Mapping	Compatible 8/16-Bit Panel Type	8/16-bit Panel P8 Mapping	8/16-bit Panel M-Signal Mapping	ENAVEE Polarity		IDE Header	CPU Fan 5V Connector	Mouse Header	Full 24-Bit Panel Connector	Power Supply Arrangement
PC/II+DXE/	L	P	M	-	V	E	F	H	J	K	S	-	a	b	c	d	e	f	g	h	j	k	n	-	t	u	v	w	r
PC/II+DXE/	0	4	1	-	2	3	3	1	0	1	3	-	0	0	2	0	1	0	0	1	0	0	0	-	1	1	1	1	6

L=0 Connector System used is 96-pin DIN (right-angle) connector and ISA header
P=4 66 MHz Intel DX4 Processor
M=1 4 MB DRAM Soldered
V=2 Video with 2 MB Video DRAM, +3.3V panel interface
E=3 Ethernet 10Base-T & AUI with Filter/Transformer and on-board Header
F=1 8 MB Flash Array Soldered
H=1 Flash Disk Socket
J=0 No SCSI-2
K=1 Real-Time Clock & Battery
S=3 2 Serial 16550 RS-232 Channels and one 2-wire BIOS RS-232 channel; includes transceivers
a=0 L1 Cache is Write-Back
b=0 SCSI Configuration is ignored when J=0
c=2 Watchdog is Installed & Enabled by H/W
d=0 IDE Cable Select is Not Grounded at Host
e=1 ISA IRQ10 is mapped to IRQ15
f=0 ISA DACK16# is mapped to DACK6# and DACK7#
g=0 ISA IRQ14# is normal
h=1 Panel Type (on J901) is Color TFT 9/12-Bit
j=0 Panel pin P8 (on J901) is signal P12
k=0 Panel pin M (one J901) is signal M
n=0 ENAVEE Polarity is Active Low
t=1 IDE 2x22 2mm Pin Header installed for IDE support
u=1 FAN Connector (5v– Molex type – 1.25 mm pitch) installed for CPU Fan use
v=1 Separate Mouse Header (1x2 .100 inch Header) installed
w=1 Separate 24-Bit Panel Connector 2x18 Pin Header (J002) installed, full 8-24-bit panel support
r=6 Dual +5V & +3.3V Supplies with both +3.3v connector J003, and +5v connector J906

10.3 PC/II+dxe Order Options

Options are listed in the following sub-sections, in alphabetical order of OPTION LETTER.

The following options are given below:

Option a CACHE Memory Bus Protocol Option
Option b SCSI Assignment
Option c Watchdog Enable
Option d IDE Cable Select
Option E Ethernet Option
Option e ISA IRQ10 Mapping
Option F Flash Array
Option f ISA DACK16# Mapping
Option g ISA IRQ14 Mapping
Option H Flash Disk-on-Chip® Socket
Option h Compatible 8/16-bit Panel Type
Option J SCSI
Option j 8/16-bit Panel P8 Mapping
Option K Real-Time Clock & Battery
Option k 8/16-bit Panel M-signal Mapping
Option L 96-pin & ISA Connector System
Option M Memory
Option n ENAVEE Polarity
Option P Processor
Option r Power Supply Arrangement
Option S Serial Channels
Option t IDE
Option u Cpu Fan (5v) Connector (J001)
Option V Video
Option v Mouse Header (JP05)
Option w Full 24-bit Panel Connector (J002)

10.3.1 Option a – CACHE Memory (L1) Bus Protocol Option

Cache is WRITE-BACK	0
Cache is WRITE-THROUGH	1

NOTES. See Option "a" in section 4.2, page 20.

10.3.2 Option b – SCSI Assignment

SCSI is configured as Primary Controller, or no SCSI device selected	0
SCSI is configured as Secondary Controller	1

NOTES. See Option "b" in section 4.2, page 20.

10.3.3 Option c – Watchdog Enable

NOT INSTALLED NO Watchdog Jumper Installed – Watchdog is Permanently Disabled	0
INSTALLED, HARDWARE DISABLED Watchdog Jumper Installed, but Jumper Socket is NOT installed – Watchdog is Disabled on the Shipped board. To Enable the watchdog, insert a jumper socket on JP01, and enable the watchdog by calling the Enable Watchdog BIOS function.	1
INSTALLED, HARDWARE ENABLED, SOFTWARE DISABLED Watchdog Jumper Installed, and Jumper Socket is Installed – Watchdog is ready to be used. As shipped, the BIOS will initially leave the watchdog in disabled state. TO use Watchdog, call the Enable Watchdog BIOS function.	2

NOTES. See Option "c" in section 4.2, page 21. Also refer to jumper JP01 on page 19.

10.3.4 Option d – IDE Cable Select

IDE Cable Select is not grounded at the host (on the Cpu board)	0
IDE Cable Select is grounded at the host (on the Cpu board)	1

NOTES. See Option "d" in section 4.2, page 21.

10.3.5 Option E – Ethernet

NO Ethernet	0
Ethernet 10BASE-T with Filters & Transformer, and Header (J903)	1
Ethernet AUI with Filters & Transformer, and Header (J903)	2
Ethernet 10BASE-T & AUI with Filters & Transformers, and Header (J903)	3

10.3.6 Option e – ISA IRQ10 Mapping

Normal, ISA IRQ10 is IRQ10	0
ISA IRQ10 is IRQ15	1

NOTES. See Option "e" in section 4.2, page 21.

10.3.7 Option F – Flash Array

NO User Flash Array	0
2MB User Flash Array, soldered	1
4MB User Flash Array, soldered	2

8MB User Flash Array, soldered	3

10.3.8 Option f – ISA DACK16# Mapping

ISA DACK16# is DACK7# and DACK6#	0
ISA DACK16# is MASTER# and DACK6#	1

NOTES. See Option "f" in section 4.2, page 21.

10.3.9 Option g – ISA IRQ14 Mapping

Normal, ISA IRQ14 is IRQ14	0
ISA IRQ14 is DRQ7	1
ISA IRQ14 is DRQ6	2

NOTES. See Option "g" in section 4.2, page 21.

10.3.10 Option H – Flash Disk-on-Chip® Socket

NO Flash Disk Socket	0
Flash Disk Socket for User-supplied Disk-on-Chip module	1

10.3.11 Option h – Compatible 8/16-bit Panel Type

Panel Type on DIN 96-pin Connector is Monochrome SS 8-Bit	0
Panel Type on DIN 96-pin Connector is Color TFT 9/12-Bit	1
Panel Type on DIN 96-pin Connector is Color STN Ext 4-Bit Packed	2

NOTES. See Option "h" in section 4.2, page 22, for a description of this option; Also, see section 0 for a description of the connector signals for each 8/16-bit option panel. This option does NOT affect the 24-bit panel interface connector, which supports all panel types. Use 0 if no Video configured.

10.3.12 Option J – SCSI

NO SCSI Bus	0
SCSI-2 Bus Controller; bus is pulled out to the Peripheral I/O connector	1

NOTES. Before ordering, Please contact Megatel for information on SCSI.

10.3.13 Option j – 8/16-bit Panel P8 Mapping

DIN 96-pin Connector pin P8 is signal P12	0
DIN 96-pin Connector pin P8 is signal ENAVEE	1

NOTES. See Option "j" in section 4.2, page 23. Use 0 if no Video configured. When P8 is ENAVEE, the polarity of this signal is either active low or active high - see option "n".

10.3.14 Option K – Real-Time Clock & Battery

NO Real-Time Clock	0
Real-Time Clock with Battery Backup is installed	1

NOTES. The Real Time Clock's RAM holds BIOS system configuration data; when not installed, the configuration data is hard-coded into the BIOS for the user. Contact Megatel Engineering for details on how to order hard-coded BIOS configuration.

10.3.15 Option k – 8/16-bit Panel M-signal Mapping

DIN 96-pin Connector pin M is signal M	0
DIN 96-pin Connector pin M is signal ENAVEE	1

NOTES. See Option "k" in section 4.2, page 23. Use 0 if No Video configured. When M is ENAVEE, the polarity of this signal is either active low or active high - see option "n".

10.3.16 Option L – 96-pin I/O & ISA Connector System

96-pin DIN (right-angle) connector, ISA header	0
96-pin & ISA tall headers (for top-mounted QTB)	1
96-pin & ISA sockets (for bottom-mounted QTB)	2
96-pin DIN (right-angle) connector, no ISA connector	3
96-pin header, no ISA connector	4
96-pin stackthrough, ISA sockets, ALL on top	5
Custom connectors	7

NOTES. J901 = 96-pin connector, J902 & J905 are ISA connectors. Specify Custom for any other option including omitting one or more connectors. Refer to section 7.3 on page 33 for connector descriptions.

10.3.17 Option M – Memory

DRAM 4 MB, soldered	1
DRAM 8 MB, soldered	2
DRAM 16 MB, soldered	3
DRAM 32 MB, soldered	4

10.3.18 Option n – ENAVEE Polarity

ENAVEE is Active Low	0
ENAVEE is Active High	1

NOTES: Affects interface connector pins J002.31, DIN96.A3(see Option "J") and DIN96.A5(see Option "k"); Select Active Low is you plan to use the compatible video interface on the 96-pin DIN connector.

10.3.19 Option P – Processor

INTEL DX4 - 100 MHz, Bus 33 MHz, soldered	1
AMD DX4 - 100 MHz, Bus 33 MHz, soldered	2
AMD DX5 - 133 MHz, Bus 33 MHz, soldered	3
INTEL DX4 - 66 MHz, Bus 33 MHz, soldered	4
INTEL DX4 - 50 MHz, Bus 16 MHz, soldered	5
INTEL DX4 - 33 MHz, Bus 16 MHz, soldered	6

NOTES: Air flow is recommended with a processor operating above 66 MHz. See Option u.

10.3.20 Option r – Power Supply Arrangement

Single +5v 5% Supply; +5v supplied through J901 power pins; +3.3v generated using on-board linear regulator	1
Single +5v 5% Supply; +5v supplied through J901 power pins; +3.3v generated by on-board switching power supply	2
Dual +5v 5% and +3.3v 5% supplies; +5v supplied through J901 power pins; +3.3v supplied through J003 power pins	3
Single +5v 5% Supply; +5v supplied through J906 power pins; +3.3v generated using on-board linear regulator	4
Single +5v 5% Supply; +5v supplied through J906 power pins; +3.3v generated by on-board switching power supply	5
Dual +5v 5% and +3.3v 5% supplies; +5v supplied through J906 power pins; +3.3v supplied through J003 power pins	6

NOTES. See Option "r" in section 4.2, page 24, for more information.

10.3.21 Option S – Serial Channels

COM1 (1) 16550 Serial Port COM1 with RS232 receivers/drivers (note- basic board always includes one serial channel)	1
COM1, COM2 (2) 16550 Serial Ports COM1 & COM2 with RS232 receivers/drivers	2
COM1, COM2, COM4 (2) 16550 Serial Ports COM1 & COM2 with RS232 receivers/drivers; and a 2-Wire BIOS Serial Port COM4 with RS232 receiver/driver	3

10.3.22 Option t – IDE

NO IDE	0
IDE, with on-board 2x22 2mm Pin Header (J904)	1

10.3.23 Option u – Cpu Fan (5v) Connector (J001)

NO Fan Connector	0
FAN Connector (5v- Molex type - 1.25 mm pitch)	1
Custom 1x2 2MM Connector	C

NOTES: Air flow is recommended with a processor operating above 66 MHz.

10.3.24 Option V – Video

NO Video	0
Video Option with +5V Panel/CRT Interface. Includes 2MB Video Memory; CRT and 8/16-bit panel interfaces are pulled to the Peripheral I/O Connector; 24-bit panel interfaces are pulled to a separate 24-bit panel connector.	1
Video Option with +3.3V Panel/CRT Interface. Same features as above.	2

10.3.25 Option v – Mouse Header (JP05)

NO Mouse Header	0
Mouse Header (1x2 .100 inch Header)	1

10.3.26 Option w – Full 24-bit Panel Connector (J002)

NO 24-bit Panel Connector (J002)	0
24-Bit Panel Connector 2x18 Pin Header (J002)	1
Custom 24-bit Panel Connector	C

NOTES: this connector is an alternative 8-bit, 16-bit or 24-bit panel interface to the 8/16-bit panel interface provided by J901. The interface on J901 provides a compatible option panel interface that is limited to 8-bit or 16-bit panels. Only one (1) panel may be attached regardless of whether either or both J901 and J002 are ordered. Analog video devices (CRT) are attached using J901 and multiplex with the 8/16-bit Panel interface on J901 (software selectable).

11 Service Information

If you feel your board requires service, Megatel Service Department will do all it can to get you up and running – quickly.

If you purchased your board from a Distributor:
Our distributors are technically capable and will help you to determine and correct your problem. Since your proof of purchase was obtained from the Distributor, please return your board to them. Please follow their instructions for returning your board for service.

If you purchased your board directly from Megatel:
Please Call or Fax to Megatel's Service Department prior to shipping, to receive your RMA# (Return Materials Authorization number). You may also submit a request for an RMA# from our Website http://www.metatel.ca. Boards that do not have RMA#s will not receive priority. To receive an RMA#, you will be required to provide the following information:

1. Company Name
2. Board Model Number or Product Order Number
3. Board Serial Number
4. Description of the Problem
5. Purchase Order Number

Special Shipping Instructions
Along with the information on the Megatel SERVICE FORM (see next page), please include the following on one of your commercial invoices:

1. The value of the board(s) – this value must match the invoice(s) we sent with the boards
2. A copy of the invoice(s) we sent with the boards (Proof of Purchase)
3. Be sure to state one of the following
   a) "Canadian Goods Being Returned for Repair"
   b) "Canadian Goods Being Returned for Warranty Repair"
   c) "Canadian Goods Being Returned"

One copy of the above documents is to be placed inside the shipping box and one copy is to be placed on the outside of the shipping box (marked for CUSTOMS). Other products (i.e. disk drives, LCD panels, etc.) that were not purchased from Megatel, but will be used as part of the servicing of the returned board, must be shipped separately and listed in the Megatel SERVICE FORM (next page) under "Equipment Sent Separately" heading. Products not purchased from Megatel should be shipped under a temporary import license of the maximum time limit.

Send PREPAID to the SERVICE DEPT. at:

MEGATEL COMPUTER CORPORATION
125 WENDELL AVENUE
WESTON, ONTARIO
M9N 3K9 CANADA

Our harmonized Number: 8471.92.00

Call us at +1 416 245-2953 between the hours of 9am to 5pm EST or send a Fax to +1 416 245-6505.

Megatel SERVICE FORM

PRIOR TO SHIPPING: : Please call Megatel to receive your RMA#. Only boards sent with an RMA# will be given priority. This RMA# must appear on all paper work and be clearly marked on the outside of the shipping box.

RMA#: _____

Date Called: _____

Your Company Name: _____

Your Contact Name: _____

Your Company Address:

Ship To: _____ **Bill To:** _____

Your Telephone Number: _____ **Extension:** _____

Your Fax Number: _____ **Extension:** _____

Equipment You are Sending to Us: Pleasefill in the following as completely and accurately as possible

Product #	Serial #	Description of the Problem

Purchase Order Number for this Return _____

Equipment Sent Separately

Courier	Waybill#	Description (include Model#, Serial#)

Courier Company to be Used for Returning this Shipment: Please Circle or Check One

FEDEX	EMERY	UPS AIR	PUROLATOR	ALPHA	TRANS	BAISLEY

OTHER _____

Special Instructions/Comments You have for us: _____

12 PC/II+dxe Physical Specifications

The physical size of the PC/II+dxe is compliant with the Megatel 4x4Family Specification. The size is 3.937 x 3.937 inches (100.0 x 100.0 mm). In the diagram, all dimensions are in MILS (1/1000'ths of an INCH).

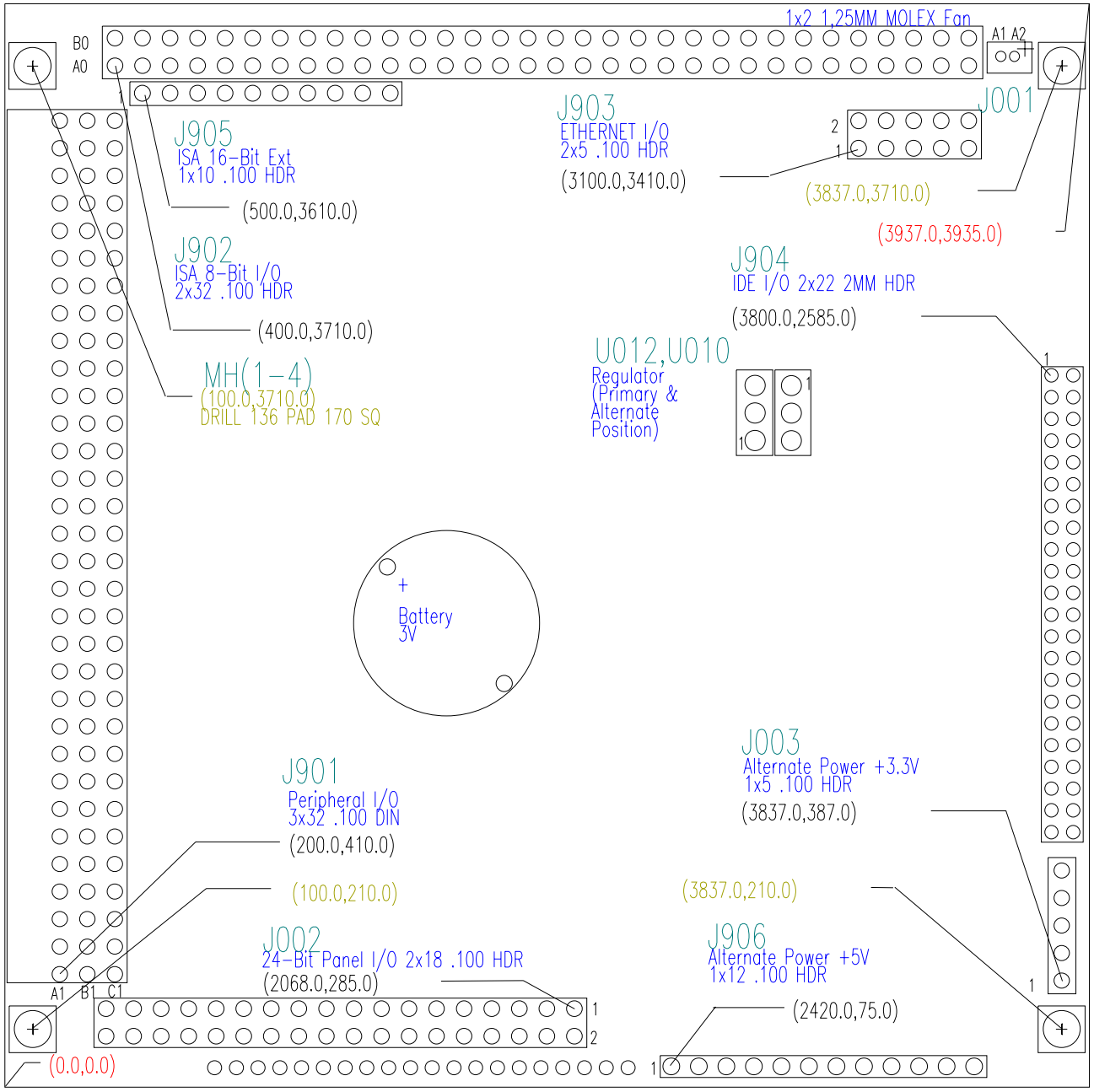


Figure 10 PC/II+dxe Physical Dimensions Diagram (v2.10)