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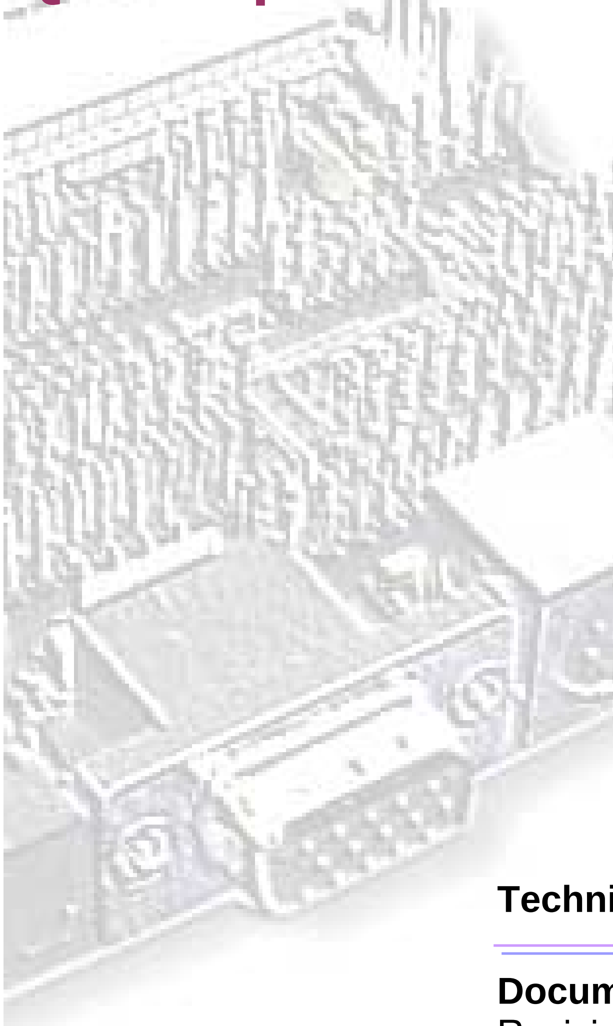
QTB/Dxp



Side-Mount Accessory I/O Transition Board

Interface for Megatel 104Family CPU Boards

Technical Reference Manual

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QTB/Dxp
Side-Mount I/O Transition Board

megatel
104Family

Product Brief

The **QTB/Dxp** board is an accessory I/O board that mates with a PC/II-104 family CPU board (such as the PC/II+dx or PC/II+p) side-by-side, extending the CPU board to provide standard I/O connection to the CPU board's peripheral I/O. The QTB/Dxp utilizes the right-angle Mass I/O connector to mate with a PC/II-104 family CPU board. It is small and rugged, and contains standard AT peripheral connectors and headers for all I/O peripherals contained on the CPU board to which it connects. The board can be ordered with the connectors populated as required by a user's application.

Features

- Megatel QTB/Dxp Board with Right-Angle plug IEC-style mass I/O connector to mate with Megatel PC/II+dx , PC/II+p and other CPU boards in the PC/II-104 family
- All I/O interface connectors and terminations are user-selectable options for all volume orders
- Standard AT type connectors are end-mounted for Keyboard, Mouse, Video VGA, and Ethernet 10Base-T, and side-mounted for USB
- LCD panel header (24-bit interface)
- USB dual-stacking two-port connector, or single port connector, with ESD protector
- IDE 40-pin (.100) and 44-pin (2mm) headers, for Ultra DMA modes
- SCSI 50-pin header, with active terminator option
- ETHERNET 10Base-T RJ45 connector
- ETHERNET AUI & Inter-Board headers
- Keyboard & Mouse (MiniDIN) Connectors
- One to four 10-pin Serial Communication Port Headers
- Parallel Port header, with EMI filter option
- Floppy Disk header
- Reset Switch (Straight-Up or Right-Angle)
- Power (System & AUI)
- Miscellaneous header

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Revision List Page

REVISION MT002110a 2000/07/24
Release Version for Qtb/Dxp v3.00

This version of MT002110a documents version v3.00 of the Qtb/Dxp PCB. Electrically and mechanically, v3.00 is identical to v2.1 of the PCB. Changes to v3.00 include the provision of additional termination options for the parallel port to support ECP/EPP more fully, additional IDE termination to support the Ultra DMA modes available on some members of the 104Family of CPU boards, and support for EMI/filtering for USB that is available on some 104Family CPU boards. Changes to component layout include providing additional clearance between the serial headers, and provision of analog planes as needed. The SCSI 25-pin header was removed; the 50-pin SCSI header provides a full SCSI interface.

In this version of MT002110a, all of the Qtb/Dxp population options are now documented. Virtually all options also have a CUSTOM setting which can also be specified by you (the customer). There are some special notes which should be observed when configuring this board. The two variants of the Reset Switch physically overlay each other on the board, and may not be selected at the same time. The Mass I-O connector may or may not be selected, and may be selected as either 5X11 or 5X22 variants. If the Mass I-O connector is not selected, then the local mini-power header will be populated by default to supply on-board needs for +5V; otherwise, +5V is supplied to the Qtb/Dxp board through the Mass I-O connector from the CPU board. In no case should +5V be supplied TO the CPU board from the Qtb/Dxp board, and if a specific configuration would cause this to happen, then the source for +5V for both the CPU board and the Qtb/Dxp board should be one and the same.

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1 Introduction

Megatel 104Family Cpu boards can be attached to peripherals by user-supplied cabling that mates directly with the on-board Mass I/O Connector and/or Ethernet Header.

Megatel also provides an economical transition board set (Qtb/Dxp) for this family of boards. The transition cards are compatible electrically with prior QTB boards, and pull all Cpu board signals to industry-standard connectors and headers.

The QTB/dxp transition board mates side-by-side with the 104Family CPU board, using both of the CPU board's Mass I/O connectors and an optional cable to the CPU board's Ethernet header. The CPU board in this configuration uses the AMP Z-PACK right-angle receptacle connectors for both of the connectors corresponding to the QTB's J901 (section 5.1) and J901 (section 5.1) connectors; the QTB/Dxp uses the AMP Z-PACK right-angle plug versions of these connectors for J901 and J902.

The QTB/dxp board is approximately 3.775 by 2.95 inches, and mates to the CPU board on the long side. It is supplied by power from +5V power pins on the Mass I/O connector which are sourced by the CPU card. An on-board power connector for +5V is also available to supply on-board +5V needs when no Mass I-O connector power is available, or when additional sourcing for +5V to the Qtb/Dxp is required. When both +5V from the Mass I-O connectors and from the on-board Power Header are both present at the same time, then they must be sourced from the same supply. Please refer to Electrical Specifications for additional information.

Connectors and Headers provided on the QTB/dxp board include the following:

- **Cpu board interface connectors**
- **Power (+5V, & +12V for Ethernet AUI)**
- **Serial – 1 to 4 ports**
- **Parallel port for ECP/EPP**
- **LCD panel (24 Bit)**
- **VGA**
- **Keyboard & Mouse (MiniDIN)**
- **Ethernet AUI**
- **Ethernet 10Base-T**
- **SCSI (50-pin)**
- **IDE 40-pin (.100) and 44-pin (2mm) for Ultra DMA**
- **Floppy**
- **USB (Dual & Single Stacking)**
- **USB Header**
- **Miscellaneous**

The QTB/dxp also contains an active termination circuit for the SCSI bus, using Dallas Semiconductor DS2107 active terminators. Jumper JP01 on the circuit board can be used to disable the terminator. Disabling the terminator (inserting the shunt) causes it to be electrically removed from the host end of the SCSI bus when, for example, you wished to physically insert the host into the middle of the SCSI bus. Without the shunt installed, the on-board host termination is active.

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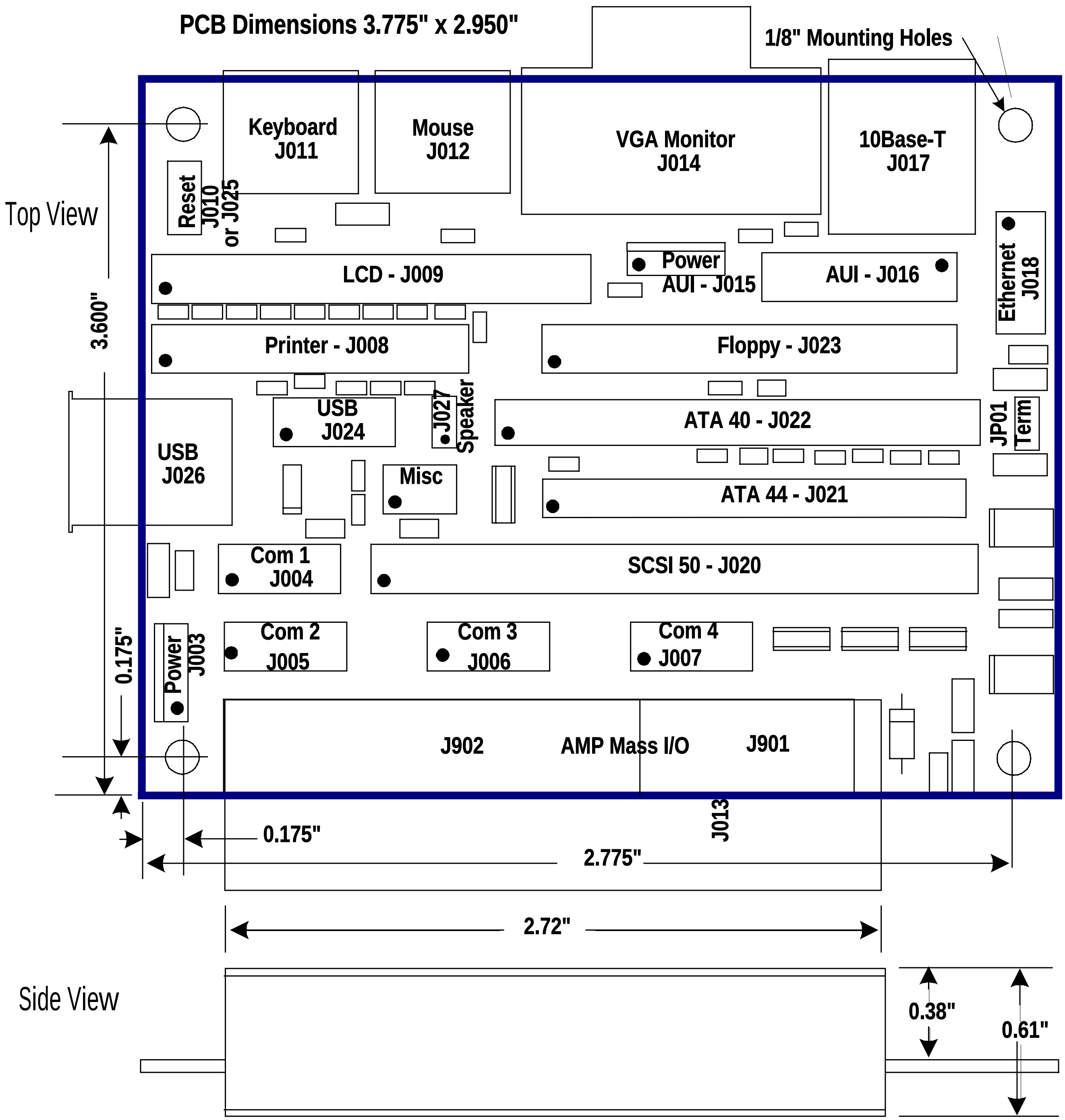
2 Board Layout

This diagram applies to Qtb/Dxp v3.00 PCB.



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3 Settings

3.1 Jumper Settings

Refer to the Qtb/Dxp Component Placement diagram. All jumpers are on the TOP side of the board.

Jumper Settings

JUMPER	SETTING	SELECTED OPTION	COMMENT
JP01:	closed (shunt installed)	DISABLE TERMINATOR – SCSI Terminator is electrically removed from the SCSI bus	When the SCSI termination is installed on the board, then this jumper controls whether or not the terminator is to be used at the HOST interface. For example, if the HOST is to be inserted into the MIDDLE of a previously terminated bus, install the jumper (this option) to disable the terminator.
	open (shunt not installed)	ENABLE TERMINATOR – SCSI Terminator is electrically inserted into the SCSI bus	When the SCSI termination is installed on the board, then this jumper controls whether or not the terminator is to be used at the HOST interface. For example, if the HOST is inserted at the END of a SCSI bus, then remove this jumper (this option) to enable the terminator.

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4 Electrical Specifications

NOTE – +5V may be supplied to BOTH the QTB/Dxp board AND the Cpu Board. In this case, the QTB receives +5V power from both the Mass I/O interface J901 and J902 (section 5.1) and from the QTB +5V Power header (J003), and you should use the same supply source for both the CPU board and the QTB board. In no case should +5V be supplied to the CPU board FROM the Qtb/Dxp board, since the rating of the Mass I-O connector is usually insufficient for this purpose. All CPU boards have separate power connectors for this purpose.

4.1 Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
Power Supply	Digital	VCC	-0.3	6.0	V
Optional 3.3V Power Supply	Digital	VCC3		3.6	V
Optional 12V Power Supply	AUI	VAUI		13.0	V
Board Current @ +5V	(Through Mass I/O)	ICC		3500	mA
Board Current @ +3.3V	(Through Mass I/O)	ICC3		100	mA
Ambient Temperature		TA	-55	+125	°C
Storage Temperature		TS	-65	+150	°C

Warning: Operation at or beyond these limits may result in permanent damage to the board or to components attached to the board. Always operate the board at the Recommended Operating Conditions, see below.

4.2 Recommended Operating Conditions

Parameter		Symbol	Min	Typical	Max	Units
Power Supply	Digital	VCC	4.75	5.0	5.25	V
Optional 3.3V Power Supply[1]	Digital	VCC3		3.3		V
Optional 12V Power Supply[1]	AUI	VAUI		12.0		V
Board Current @ +5V	(Through Mass I/O)	ICC			3000	mA
Board Current @ +3.3V	(Through Mass I/O)	ICC3			50	mA
Operating Ambient Temperature		TA	0		70	°C
Storage Ambient Temperature		TS	-55		+125	°C
Humidity	(Untested)	HA	10		90	% RH

NOTES

[1] VCC3 (+3.3V) is sourced by the Mass I/O Connector from the CPU board, and is pulled to the 6-pin Miscellaneous Header J013 (section 5.9). VAUI (+12V) is optionally sourced by the on-board 4-Pin Ethernet AUI Power Header J015 (section 5.11), and is tied directly to the 16-pin Ethernet AUI Header J016 (section 5.12).

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5 Connectors & Headers

Table 1 List – QTB/dxp Side-Mount Connectors

Ref	Connector / Header Description	See Section
J901, J902	Mass I/O Board Connector – 5x22 and 5x11 AMP Z-PACK 2mm HM Right-angle plugs	5.1
J003	4-Pin System Power (+5v, Gnd, Gnd, N/C)	5.2
J004	COM1 Header – 10-pin 2x5 (0.100" pitch) Header	5.3
J005	COM2 Header – 10-pin 2x5 (0.100" pitch) Header	5.3
J006	COM3 Header – 10-pin 2x5 (0.100" pitch) Header	5.3
J007	COM4 Header – 10-pin 2x5 (0.100" pitch) Header	5.3
J008	Printer Parallel Port Header – 26-Pin 2x13 (0.100" pitch) Header	5.4
J009	Video Panel Header – 36-pin 2x18 (0.100" pitch) Header	5.5
J010	Reset Switch – 3-Pin Standard Straight-Up	5.6
J011	Keyboard Connector – MiniDIN-6 PS/2-style Keyboard Connector (at card edge)	5.7
J012	Mouse Connector – MiniDIN-6 PS/2-style Mouse Connector (at card edge)	5.8
J013	Miscellaneous Header – 6-pin 2x3 (0.100" pitch) Header	5.9
J014	Video VGA Monitor Connector – DSUB-15 Receptacle (at card edge)	5.10
J015	Ethernet AUI Power Connector – 4-pin (+12v, Gnd, Gnd, N/C)	5.11
J016	Ethernet AUI Header – 16-pin 2x8 (0.100" pitch) Header	5.12
J017	Ethernet 10Base-T Connector – RJ-45 Connector (at card edge)	5.13
J018	Ethernet Board Header – 10-pin 2x5 (0.100" pitch) Header	5.14
J020	SCSI Header – 50-pin 2x25 (0.100" pitch) Header	5.15
J021	IDE/ATA Header – 44-pin 2x22 (2mm pitch) Header	5.16
J022	IDE/ATA Header – 40-pin 2x20 (0.100" pitch) Header	5.17
J023	Floppy Connector – 34-pin 2x17 (0.100" pitch) Header	5.18
J024	USB Header – 10-pin 2x5 (0.100" pitch) Header	5.19
J025	Reset Switch – 4-pin Right-angle SPST Momentary Switch	5.20
J026	USB Connector – 8-pin Dual Stacking Connector (at card edge)	5.21
J027	Speaker Header – 2-pin (0.100" pitch) Speaker-Output Header	5.22
JP01	SCSI Terminator Jumper – Enable (Jumper Present) or Disable (Jumper Removed)	

NOTES
[1] *Either J010 (section 5.6) or J025 (section 5.20), will be populated, but not both.*
[2] *Header J018 (Section 5.14) is cabled to the board containing the Ethernet controller (for example, the CPU board).*

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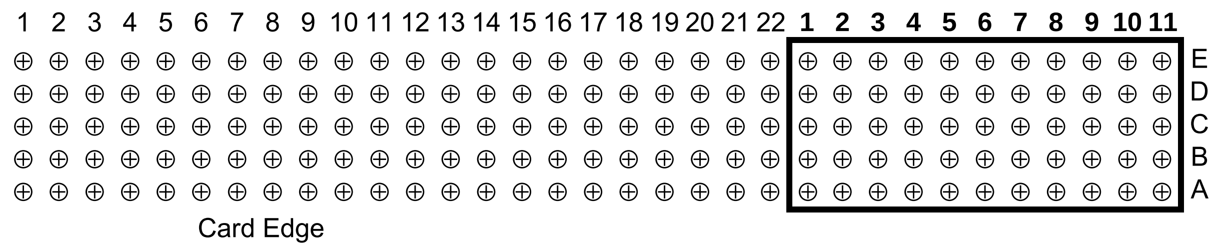
5.1 J901,J902 – Mass I/O Board Connectors

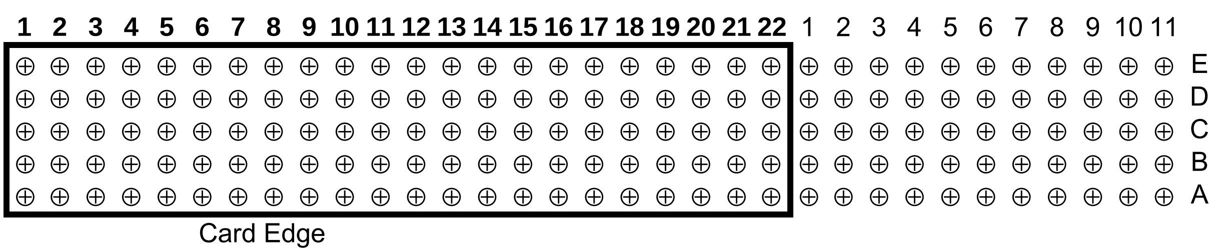
All peripheral I/O, with the exception of J018 (Ethernet, section 5.14), is pulled from the CPU board to a 5 X 33 2mm grid Mass I/O Connector, which interfaces to the QtbDxp board. The Mass I/O Connector is normally provided using two separate connectors, J901 (section 5.1), a 5 X 11 2mm connector, and J902 (section 5.1), a 5 X 22 2mm connector. Both of the CPU board and the Qtb/Dxp boards can be ordered with either or both of these two connectors installed, although both would be installed in a typical case. In addition, both of these boards can be shipped with any combination of user-specified 2mm headers.

Figure 1 MASS I/O J901 (Rows A, B, C, D and E) – 5 X 11 2mm HM Connector



NOTES
[1] *Top (component) view is shown. This is the view when facing either a straight connector from the top, or a right-angle connector facing the outer side (the mating side). Rotate the diagram above clockwise 90 degrees to obtain the diagram of the connector on the top side of the board (in which case the card edge is to the right).*

Figure 2 MASS I/O J902 (Rows A, B, C, D and E) – 5 X 22 2mm HM Connector



NOTES
[1] *Top (component) view is shown. This is the view when facing either a straight connector from the top, or a right-angle connector facing the outer side (the mating side). Rotate the diagram above clockwise 90 degrees to obtain the diagram of the connector on the top side of the board (in which case the card edge is to the right).*

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Table 2 Pinout – J901 Mass I/O – 5 X 11 2mm HM Connector

PIN GROUP	POS	ROW e	ROW d	ROW c	ROW b	ROW a
V1-VIDEO1 V1-CRT1	1	V1-R	V1-G	V1-B	V1-HSYNC	V1-VSYNC
A1-IDE1	2	A1-DD7	A1-DD8	A1-DD6	A1-DD9	A1-DD5
A1-IDE1	3	A1-DD10	A1-DD4	A1-DD11	A1-DD3	A1-DD12
A1-IDE1	4	A1-DD2	A1-DD13	A1-DD1	A1-DD14	A1-DD0
A1-IDE1	5	A1-DD15	A1-DMARQ	A1-DIOW#	A1-DIOR#	A1-IORDY
A1-IDE1	6	A1-DMACK#	A1-INTRQ	A1-IOCS16#	A1-DA1	A1-DA0
A1-IDE1 S1-SCSI	7	A1-DA2	A1-CS0#	A1-CS1#	S1-REQ#	S1-MSG#
S1-SCSI	8	S1-C/D#	S1-I/O#	S1-RST#	S1-ATN#	S1-AKN#
S1-SCSI	9	S1-BSY#	S1-SEL#	S1-DP#	S1-D0#	S1-D1#
S1-SCSI	10	S1-D2#	S1-D3#	S1-D4#	S1-D5#	S1-D6#
POWER	11	S1-D7#	GND	GND	+5V	+5V

Table 3 Pinout – J902 Mass I/O – 5 X 22 2mm HM Connector

PIN GROUP	POS	ROW e	ROW d	ROW c	ROW b	ROW a
L1-PANEL	1	L1-PD23	L1-PD22	GND	L1-PD21	+5V
L1-PANEL	2	L1-PD20	L1-PD19	L1-PD18	L1-PD17	L1-PD16
L1-PANEL	3	L1-PD15	L1-PD14	L1-PD13	L1-PD12	L1-PD11
L1-PANEL	4	L1-PD10	L1-PD9	L1-PD8	L1-PD7	L1-PD6
L1-PANEL	5	L1-PD5	L1-PD4	L1-PD3	L1-PD2	L1-PD1
L1-PANEL	6	L1-PD0	L1-SHFCLK	L1-LP	L1-FLM	L1-ENAVEE
L1-PANEL MS-SPEAKER	7	L1-ENAVDD	L1-M	L1-ACT	L1-ENABKL	MS-SPKOUT
MR-RESET MISCELLANEOUS K1-KEYBOARD	8	MR-RSTSW	PWRGOOD	K1-DAT	K1-CLK	+3.3V
M1-MOUSE P1-PARALLEL1 – LPT1	9	M1-DAT	M1-CLK	P1-STB#	P1-AFD#	P1-D0
P1-PARALLEL1 - LPT1	10	P1-ERR#	P1-D1	P1-INIT#	P1-D2	P1-SLIN#
P1-PARALLEL1 - LPT1	11	P1-D3	P1-D4	P1-D5	P1-D6	P1-D7
P1-PARALLEL1 - LPT1 C1-SERIAL1 - COM1	12	P1-AKN#	P1-BUSY	P1-PE	P1-SLCT	C1-DCD
C1-SERIAL1 - COM1	13	C1-DSR	C1-RXD	C1-RTS	C1-TXD	C1-CTS
C1-SERIAL1 - COM1 C2-SERIAL2 - COM2	14	C1-DTR	C1-RI	C2-DCD	C2-DSR	C2-RXD
C2-SERIAL2 - COM2	15	C2-RTS	C2-TXD	C2-CTS	C2-DTR	C2-RI
C3-SERIAL3 - COM3	16	C3-DCD	C3-DSR	C3-RXD	C3-RTS	C3-TXD
C3-SERIAL3 - COM3 C4-SERIAL4 - COM4	17	C3-CTS	C3-DTR	C3-RI	C4-DCD	C4-DSR
C4-SERIAL4 - COM4	18	C4-RXD	C4-RTS	C4-TXD	C4-CTS	C4-DTR
C4-SERIAL4 - COM4	19	C4-RI	U1-D+	U1-D-	U2-D+	U2-D-
F1-FLOPPY1	20	F1-DENSL0#	F1-INDEX#	F1-MTR0#	F1-DS1#	F1-DS0#
F1-FLOPPY1	21	F1-MTR1#	F1-DIR#	F1-STEP#	F1-WDATA#	F1-WGATE#
F1-FLOPPY1	22	F1-TRK0#	F1-WP#	F1-RDATA#	F1-HDSEL#	F1-DKCHG#

5.2 J003 – +5V Power Header

Table 4 Pinout – J003 – +5V Power Header

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
+5V	1	+5V	POWER +5V
GND	2	Ground	Ground
GND	3	Ground	Ground
N/C	4	N/C	Not connected

J003 is a mini power 4-pin connector.

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5.3 J004,J005,J006,J007 – Serial COM1,2,3,4 Headers

The RS-232E levels on pins 1-8 are in the functional ON (spacing) state when the interchange line level is greater than +3V, and in the functional OFF (marking) state when the interchange line level is less than -3V. The RS-232E levels are restricted to a maximum of 25V in magnitude, and are typically in the range of magnitudes of from 5V to 15V when the terminator load resistance is in the range between 3000 ohms and 7000 ohms.

The RS-232E signals are converted on the CPU board to logic level signals using an RS-232E line driver. The line driver typically inverts the RS-232E voltage level when it converts it to a TTL logic level signal; the UART re-inverts the signal again, so that a modem status bit, for example, will indicate a value of 1 when the TTL level signal is at logic 0.

Typically, Megatel CPU boards utilize ADM211E line drivers. For these line drivers, a functional ON RS-232E signal (>+3V) is converted to a logic 0 level, and a functional OFF RS-232E signal (<-3V) is converted to a logic 1 level. Driving a typical EIA-232-E load, the output voltage swing is ±9 V. Driving worst case loads, the output voltage swing is no less than the RS-232E minimum of ±5 V. Voltage slew of 30V/µs meets the RS-232E requirement.

Please refer to the datasheet for the serial UART component used by the CPU board, for more information (the UART type will be specified in the CPU board's Technical Reference Manual).

J004, J005, J006 and J007 are 10-pin 2X5 (0.100" pitch) headers.

Table 5 Pinout – J004, J005, J006, J007 – Serial COM1,2,3,4 Interface Headers

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION (RS-232E)
C1-DCD	1	Data Carrier Detect	This RS-232E input pin is tied to the local modem. The ON condition on that circuit is presented when the modem has detected a good signal (or carrier signal). The OFF condition indicates that no signal is being received or that the received signal is unsuitable for demodulation. The CPU can monitor the status of the DCD signal by reading bit 7 of Modem Status Register (MSR).
C1-DSR	2	Data Set Ready	This RS-232E input pin is tied to the local modem. The ON condition notifies the UART that the modem is in its ready state. The OFF condition notifies the UART that the modem is not in its ready state. During the OFF condition, the UART can present the Data Terminal Ready signal, and can respond to the Ring Indicator signal, but all other inputs should be ignored. The CPU can monitor the status of the DSR signal by reading bit-5 of Modem Status Register (MSR).
C1-RXD	3	Receive Data	This RS-232E input pin carries the serial receive data
C1-RTS	4	Request to Send	This RS-232E output pin is tied to the local modem. The ON condition notifies the modem to enter (or remain in) the transmit (CTS ON) mode. The OFF condition notifies the modem to enter (or remain in) the non-transmit (CTS OFF) mode. The CPU can program this signal by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS signal to inactive mode (high).
C1-TXD	5	Transmit Data	This RS-232E output pin carries the serial transmit data.

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PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION (RS-232E)
C1-CTS	6	Clear to Send	This RS-232E input pin is tied to the local modem. The ON condition notifies the CPU that the modem is in transmit mode and is ready to transmit, or is transmitting data. The OFF condition notifies the CPU that the modem is not in transmit mode and that the CPU should not transmit serial data to the modem. The CPU can monitor the status of the CTS signal by reading bit 4 of Modem Status Register (MSR).
C1-DTR	7	Data Terminal Ready	This RS-232E output pin is tied to the local modem. The ON condition notifies the modem that the CPU is ready to establish data communication link. The OFF condition notifies the modem that, after "in progress" transmission completes, the data communications link is to be broken, or is to remain disconnected. The CPU can be program this signal by writing to bit 0 of Modem Control Register (MCR).
C1-RI	8	Ring Indicator	This RS-232E input pin is tied to the local modem. The ON condition notifies the CPU that a ringing signal is being received on the communications channel, approximately coincident with the ON segment of the ringing cycle on the communications channel. The OFF condition is presented to the CPU at all other times. The CPU can monitor the status of the RI signal by reading bit 6 of Modem Status Register (MSR).
GND	9	Ground	Protective Ground
N/C	10	Not Connected	Not Connected

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5.4 J008 – Parallel LPT1 Header

J008 is a 26-pin 2X13 (0.100" pitch) header.

Table 6 Pinout – J008 – Parallel LPT1 Interface Header

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
P1-STB#	1	Strobe Output	This active low pulse is used to strobe the printer data into the printer. This output signal is the complement of bit 0 of the Printer Control Register.
P1-AFD#	2	Autofeed Output	This active low output causes the printer to automatically feed one line after each line is printed. This signal is the complement of bit 1 of the Printer Control Register.
P1-D0	3	Port Data - Bit-0	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-ERR#	4	Error	This active low signal indicates an error condition at the printer.
P1-D1	5	Port Data - Bit-1	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-INIT#	6	Initiate Output	This active low signal is bit 2 of the printer control register. This is used to initiate the printer when low.
P1-D2	7	Port Data - Bit-2	This bi-directional parallel data bus is used to transfer information between CPU and printer.
P1-SLIN#	8	Printer select input	This active low signal selects the printer. This is the complement of bit 3 of the Printer Control Register.
P1-D3	9	Port Data - Bit-3	This bi-directional parallel data bus is used to transfer information between CPU and printer.
GND	10	Ground	Ground
P1-D4	11	Port Data - Bit-4	This bi-directional parallel data bus is used to transfer information between CPU and printer.
GND	12	Ground	Ground
P1-D5	13	Port Data - Bit-5	This bi-directional parallel data bus is used to transfer information between CPU and printer.
GND	14	Ground	Ground
P1-D6	15	Port Data - Bit-6	This bi-directional parallel data bus is used to transfer information between CPU and printer.
GND	16	Ground	Ground
P1-D7	17	Port Data - Bit-7	This bi-directional parallel data bus is used to transfer information between CPU and printer.
GND	18	Ground	Ground
P1-AKN#	19	Acknowledge	This active low output from the printer indicates it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the PACK# input.
GND	20	Ground	Ground

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PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
P1-BUSY	21	Busy	This signal indicates the status of the printer. A high indicates the printer is busy and not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input.
GND	22	Ground	Ground
P1-PE	23	Paper End	This signal indicates that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input.
GND	24	Ground	Ground
P1-SLCT	25	Printer Selected Status	This active high output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input.
GND	26	Ground	Ground

5.5 J009 – Video Panel Header

J009 is a 36-pin 2X18 (0.100" pitch) header.

Table 7 Pinout – J009 – Panel Interface Header

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
GND	1	Ground	Ground
+5V	2	+5V	POWER +5V
L1-FPD23	3	Data Output P23	Flat panel data output P23. Active high. Output.
L1-FPD22	4	Data Output P22	Flat panel data output P22. Active high. Output.
L1-FPD21	5	Data Output P21	Flat panel data output P21. Active high. Output.
L1-FPD20	6	Data Output P20	Flat panel data output P20. Active high. Output.
L1-FPD19	7	Data Output P19	Flat panel data output P19. Active high. Output.
L1-FPD18	8	Data Output P18	Flat panel data output P18. Active high. Output.
L1-FPD17	9	Data Output P17	Flat panel data output P17. Active high. Output.
L1-FPD16	10	Data Output P16	Flat panel data output P16. Active high. Output.
L1-FPD15	11	Data Output P15	Flat panel data output P15. Active high. Output.
L1-FPD14	12	Data Output P14	Flat panel data output P14. Active high. Output.
L1-FPD13	13	Data Output P13	Flat panel data output P13. Active high. Output.
L1-FPD12	14	Data Output P12	Flat panel data output P12. Active high. Output.
L1-FPD11	15	Data Output P11	Flat panel data output P11. Active high. Output.
L1-FPD10	16	Data Output P10	Flat panel data output P10. Active high. Output.
L1-FPD9	17	Data Output P9	Flat panel data output P9. Active high. Output.
L1-FPD8	18	Data Output P8	Flat panel data output P8. Active high. Output.
L1-FPD7	19	Data Output P7	Flat panel data output P7. Active high. Output.
L1-FPD6	20	Data Output P6	Flat panel data output P6. Active high. Output.
L1-FPD5	21	Data Output P5	Flat panel data output P5. Active high. Output.
L1-FPD4	22	Data Output P4	Flat panel data output P4. Active high. Output.
L1-FPD3	23	Data Output P3	Flat panel data output P3. Active high. Output.
L1-FPD2	24	Data Output P2	Flat panel data output P2. Active high. Output.
L1-FPD1	25	Data Output P1	Flat panel data output P1. Active high. Output.
L1-FPD0	26	Data Output P0	Flat panel data output P0. Active high. Output.
L1-SHFCLK	27	Shift Clock	(SHFCLK or CL2 or SHFCLKL) This signal is the pixel clock for flat panel data. Active high. Output.
L1-LP	28	Latch Pulse	Flat Panel equivalent of HSYNC. Active high. Output.
L1-FLM	29	First Line Marker	Flat Panel equivalent of VSYNC. Active high. Output.
L1-M	30	M signal	This signal is the M-signal for panel AC drive control (may also be called ACDCLK). May also be configured as BLANK# or as Display Enable (DE) for TFT Panels. Active High. Output.

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PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
L1-ENAVEE	31	Enable VEE	(ENAVEE or ENABKL) Power sequencing controls for panel LCD bias voltage VEE, I/O.
L1-ENAVDD	32	Enable VDD	Power sequencing controls for panel driver electronics voltage VDD. I/O.
L1-ENABKL	33	Enable Backlight	(ENABKL or A27 or GP1 or DCLK or CS) This signal is the Enable Backlight output signal. It may be configured for other functions (see Chips 65550 Datasheet – Extension Registers FR0C and FR0F and pin descriptions of MCD0-15 and A26/A27 for more information). (Chips Revision 1.5 10/14/97 65550 Subject to Change without Notice). I/O.
L1-ACTI	34	Activity Indicator	(ACTI or A26 or GP0 or DDAT or CS) This signal is the Activity Indicator output. It may be configured for other functions (see Chips 65550 Datasheet – Extension Registers FR0C and FR0F and pin descriptions of MCD0-15 and A26/A27 for more information). I/O.
GND	35	Ground	Ground
+5V	36	+5V	POWER +5V

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5.6 J010 – Reset (2-Pin Straight-Up) Switch

A 3-pad connector is provided, for example to accommodate a straight-up 2-pin 200 mil reset switch, or a 2-pin 100 mil header.

J010 is a SPST momentary-contact N.O. (normally open) type of switch. The button is perpendicular to the plane of the PCB.

Either J010 or J025 (section 5.20) may be populated (but not both at the same time).

Table 8 Pinout – J010 – Reset Switch – 3 Pin Straight Up

PIN NAME	PAD#	SIGNAL NAME	SIGNAL DESCRIPTION
MR-RSTSW#	1	Manual Reset	Hard Reset Input, Active low. This signal drives the Manual-Reset Input. A logic low on this signal asserts system reset. Reset remains asserted as long as this signal is held low and for 200ms (typical; minimum 130ms) after this signal returns high. The active-low input has an internal 52kΩ pull-up resistor. It can be driven from a CMOS-logic line or shorted to ground with a switch. Leave open or connect to VCC (+5V) if unused.
MR-RSTSW#	2	Manual Reset	Hard Reset Input, Active low. This signal drives the Manual-Reset Input. A logic low on this signal asserts system reset. Reset remains asserted as long as this signal is held low and for 200ms (typical; minimum 130ms) after this signal returns high. The active-low input has an internal 52kΩ pull-up resistor. It can be driven from a CMOS-logic line or shorted to ground with a switch. Leave open or connect to VCC (+5V) if unused.
GND	3	Ground	Ground

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5.7 J011 – Keyboard Connector

J011 is a Mini DIN-6 circular connector, mounted at right angle at the edge of the card, for PS/2-style keyboards.

Table 9 Pinout – J011 – Keyboard Connector

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
K1-DAT	1	Keyboard Data	This input is the keyboard serial data line.
N/C	2	Not Connected	Not Connected
GND	3	Ground	Ground. Note : Connector case is also connected to ground
+5V	4	+5V	Power +5v
K1-CLK	5	Keyboard Clock	This output is the keyboard interface clock.
N/C	6	Not Connected	Not Connected

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5.8 J012 – Mouse Connector

J012 is a Mini DIN-6 circular connector, mounted at right angle at the edge of the card, for a PS/2-style mouse.

Table 10 Pinout – J012 – Mouse Connector

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
M1-DAT	1	Mouse Data	This input is the mouse serial data line.
N/C	2	Not Connected	Not Connected
GND	3	Ground	Ground. Note : Connector case is also connected to ground
+5V	4	+5V	Power +5v
M1-CLK	5	Mouse Clock	This output is the PS2 Mouse clock.
N/C	6	Not Connected	Not Connected

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5.9 J013 – Miscellaneous Header

J013 is a 6-pin 2X3 (0.100" pitch) header.

Table 11 Pinout – J013 – Miscellaneous

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
+3.3V	1	+3.3v	+3.3v
PWRGOOD	2	Power Good	This signal is the Power Good output signal. It pulses low for 200 ms (typical, minimum 130 ms) when triggered by RSTSW# or by a Watchdog Timer Expired event, and it remains low whenever VCC is below the reset threshold or when the RSTSW# signal input is a logic low. This output signal remains low for 200ms (typical, minimum 130 ms) after one of the following occurs: VCC rises above the reset threshold, the watchdog triggers a reset, or the RSTSW# input signal goes low to high.
MR-RSTSW#	3	Manual Reset	Hard Reset Input, Active low. This signal drives the Manual-Reset Input. A logic low on this signal asserts system reset. Reset remains asserted as long as this signal is held low and for 200ms (typical; minimum 130ms) after this signal returns high. The active-low input has an internal 52kΩ pull-up resistor. It can be driven from a CMOS-logic line or shorted to ground with a switch. Leave open or connect to VCC (+5V) if unused.
GND	4	Ground	Ground.
MS-SPKROUT	5	Speaker Output	This signal is used to control the Speaker Output and should connect to the Speaker.
+5V	6	+5V	POWER +5V

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5.10 J014 – Video DSUB-15 Connector

J014 is a 15-pin DSUB Receptacle, right-angle, for standard VGA monitors. It is side-mounted at the edge of the card.

Table 12 Pinout – J014 – Video CRT Display Interface – DSUB-15 Receptacle

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
V1-R	1	CRT Red	This Active High output signal is the RED CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm equivalent load on each pin (e.g. 75 ohm resistor on the board, in parallel with the 75 ohm CRT load).
V1-G	2	CRT Green	This Active High output signal is the GREEN CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm equivalent load on each pin (e.g. 75 ohm resistor on the board, in parallel with the 75 ohm CRT load).
V1-B	3	CRT Blue	This Active High output signal is the BLUE CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm equivalent load on each pin (e.g. 75 ohm resistor on the board, in parallel with the 75 ohm CRT load).
N/C	4	Not Connected	Not Connected
GND	5	Ground	Ground.
GND	6	Ground	Ground.
GND	7	Ground	Ground.
GND	8	Ground	Ground.
N/C	9	Not Connected	Not Connected
GND	10	Ground	Ground.
N/C	11	Not Connected	Not Connected
N/C	12	Not Connected	Not Connected
V1-HSYNC	13	Horizontal Sync	(HSYNC or CSYNC) This Active High/Low output signal is the CRT Horizontal Sync (polarity is programmable) or the "Composite Sync" for support of various external NTSC/PAL encoder chips. Note CSYNC can be set to output on the L1-ACTI pin (Mass I/O pin B - c7) or the L1-ENABKL pin (Mass I/O pin B - b7).
V1-VSYNC	14	Vertical Sync	(VSYNC or VISINT) This Active High/Low output signal is the CRT Vertical Sync (polarity is programmable) or "VSync Interval" for support of various external NTSC/PAL encoder chips.
N/C	15	Not Connected	Not Connected

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5.11 J015 – Ethernet AUI Power Header

J015 is a 4-pin Mini Power header.

Table 13 Pinout – J015 – Ethernet AUI Power Header

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
N/C	1	N/C	Not connected
GND	2	Ground	Ground
GND	3	Ground	Ground
+12V	4	+12V	POWER +12V

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5.12 J016 – Ethernet AUI Header

J016 is a 16-pin 2X8 (0.100" pitch) header.

Table 14 Pinout – J016 – Ethernet AUI Header

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
GND	1	Ground	Ground
E2-CLSN-	2	Negative Collision In	Negative Differential AUI Collision Input Line, to onboard AUI Isolation Transformer Pin 13. Connect to external DB15 connector Pin 9.
E2-CLSN+	3	Positive Collision In	Positive Differential AUI Collision Input Line, to onboard AUI Isolation Transformer Pin 10. Connect to external DB15 connector Pin 2.
E2-TRMT-	4	Negative Transmit Data	Negative Differential Manchester-encoded Transmit Data Line, 10 Mbps, from onboard AUI Isolation Transformer Pin 16. Connect to external DB15 connector Pin 10.
E2-TRMT+	5	Positive Transmit Data	Positive Differential Manchester-encoded Transmit Data Line, 10 Mbps, from onboard AUI Isolation Transformer Pin 15. Connect to external DB15 connector Pin 3.
GND	6	Ground	Ground
GND	7	Ground	Ground
E2-RCV-	8	Negative Receive Data	Negative Differential Manchester-encoded Receive Data Line, 10 Mbps, to onboard AUI Isolation Transformer (1:1) Pin 10. Connect to external DB15 connector Pin 12.
E2-RCV+	9	Positive Receive Data	Positive Differential Manchester-encoded Receive Data Line, 10 Mbps, to onboard AUI Isolation Transformer (1:1) Pin 9. Connect to external DB15 connector Pin 5.
+12V	10	+12V	POWER +12V
GND	11	Ground	Ground
GND	12	Ground	Ground
N/C	13	N/C	Not connected
N/C	14	N/C	Not connected
N/C	15	N/C	Not connected
N/C	16	N/C	Not connected

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5.13 J017 – Ethernet 10Base-T RJ45 Connector

J017 is a Telco 8-pin Jack, mounted at right-angle on the board.

Table 15 Pinout – J017 – Ethernet – 10Base-T – RJ45 Connector

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
E1-TD+	1	Positive Transmit Data	Positive Differential Manchester-encoded Transmit Data Line, 10 Mbps, from onboard 10 BASE T Isolation Transformer (1:SQRT(2)) Pin 9. Connect to external RJ45 connector Pin 1.
E1-TD-	2	Negative Transmit Data	Negative Differential Manchester-encoded Transmit Data Line, 10 Mbps, from onboard 10 BASE T Isolation Transformer (1:SQRT(2)) Pin 11. Connect to external RJ45 connector Pin 2.
E1-RD+	3	Positive Receive Data	Positive Differential Manchester-encoded Receive Data Line, 10 Mbps, to onboard 10 BASE T Isolation Transformer (1:1) Pin 14. Connect to external RJ45 connector Pin 3.
N/C	4	N/C	Not connected
N/C	5	N/C	Not connected
E1-RD-	6	Negative Receive Data	Negative Differential Manchester-encoded Receive Data Line, 10 Mbps, to onboard 10 BASE T Isolation Transformer (1:1) Pin 16. Connect to external RJ45 connector Pin 6.
N/C	7	N/C	Not connected
N/C	8	N/C	Not connected

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5.14 J018 – Ethernet Controller Header

J018 is a 10-pin 2X5 (0.100" pitch) header.

Note – this Header receives a cable attached to the CPU board. CPU board for the 104Family typically use the identical header to J018.

Table 16 Pinout – J018 Ethernet – 2x5 Pin .100 Inch R/A Header

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
E2-CLSN-	1	Negative Collision In	Negative Differential AUI Collision Input Line, to onboard AUI Isolation Transformer Pin 13. Connect to external DB15 connector Pin 9.
E2-CLSN+	2	Positive Collision In	Positive Differential AUI Collision Input Line, to onboard AUI Isolation Transformer Pin 10. Connect to external DB15 connector Pin 2.
E1-RD-	3	Negative Receive Data	Negative Differential Manchester-encoded Receive Data Line, 10 Mbps, to onboard 10 BASE T Isolation Transformer (1:1) Pin 16. Connect to external RJ45 connector Pin 6.
E1-RD+	4	Positive Receive Data	Positive Differential Manchester-encoded Receive Data Line, 10 Mbps, to onboard 10 BASE T Isolation Transformer (1:1) Pin 14. Connect to external RJ45 connector Pin 3.
E2-RCV-	5	Negative Receive Data	Negative Differential Manchester-encoded Receive Data Line, 10 Mbps, to onboard AUI Isolation Transformer (1:1) Pin 10. Connect to external DB15 connector Pin 12.
E2-RCV+	6	Positive Receive Data	Positive Differential Manchester-encoded Receive Data Line, 10 Mbps, to onboard AUI Isolation Transformer (1:1) Pin 9. Connect to external DB15 connector Pin 5.
E1-TD-	7	Negative Transmit Data	Negative Differential Manchester-encoded Transmit Data Line, 10 Mbps, from onboard 10 BASE T Isolation Transformer (1:SQRT(2)) Pin 11. Connect to external RJ45 connector Pin 2.
E1-TD+	8	Positive Transmit Data	Positive Differential Manchester-encoded Transmit Data Line, 10 Mbps, from onboard 10 BASE T Isolation Transformer (1:SQRT(2)) Pin 9. Connect to external RJ45 connector Pin 1.
E2-TRMT-	9	Negative Transmit Data	Negative Differential Manchester-encoded Transmit Data Line, 10 Mbps, from onboard AUI Isolation Transformer Pin 16. Connect to external DB15 connector Pin 10.
E2-TRMT+	10	Positive Transmit Data	Positive Differential Manchester-encoded Transmit Data Line, 10 Mbps, from onboard AUI Isolation Transformer Pin 15. Connect to external DB15 connector Pin 3.

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5.15 J020 – SCSI (50 Pin) Header

J020 is a 50-pin 2X25 (0.100" pitch) header.

Table 17 Pinout – J020 – SCSI Bus Interface – 50 pin

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
GND	1	Ground	Ground
S1-D0#	2	Data Bus Bit Signal 0	Data bit signal 0. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. S1-D1# thru S1-D8# define eight data-bit signals. Together with the S1-DP# a parity-bit signal, they form a DATA BUS. S1-D7# is the most significant bit and has the highest priority during the ARBITRATION phase. Bit number, significance, and priority decrease downward to S1-D0#.
GND	3	Ground	Ground
S1-D1#	4	Data Bus Bit Signal 1	Data bit signal 1. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
GND	5	Ground	Ground
S1-D2#	6	Data Bus Bit Signal 2	Data bit signal 2. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
GND	7	Ground	Ground
S1-D3#	8	Data Bus Bit Signal 3	Data bit signal 3. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
GND	9	Ground	Ground
S1-D4#	10	Data Bus Bit Signal 4	Data bit signal 4. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
GND	11	Ground	Ground
S1-D5#	12	Data Bus Bit Signal 5	Data bit signal 5. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
GND	13	Ground	Ground
S1-D6#	14	Data Bus Bit Signal 6	Data bit signal 6. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
GND	15	Ground	Ground
S1-D7#	16	Data Bus Bit Signal 7	Data bit signal 7. A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false. See S1-D0#.
GND	17	Ground	Ground

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PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
S1-DP#	18	Data Bus Parity	Data parity bit signal. Parity is Odd. Parity is undefined during the ARBITRATION phase. See S1-D0#.
GND	19	Ground	Ground
GND	20	Ground	Ground
GND	21	Ground	Ground
GND	22	Ground	Ground
GND	23	Ground	Ground
GND	24	Ground	Ground
N/C	25	N/C	Not connected
TERMPWR	26	Termination Power	Diode protected / transient suppressed +5V for powering SCSI terminators
GND	27	Ground	Ground
GND	28	Ground	Ground
GND	29	Ground	Ground
GND	30	Ground	Ground
GND	31	Ground	Ground
S1-ATN#	32	Attention	A signal driven by an initiator to indicate the ATTENTION condition.
GND	33	Ground	Ground
GND	34	Ground	Ground
GND	35	Ground	Ground
S1-BSY#	36	Busy	An "OR-tied" signal that indicates that the bus is being used. It may be driven by all SCSI devices that are actually arbitrating during Arbitration, driven by the initiator, target or both during Selection & Reselection, or driven by the target during all other phases.
GND	37	Ground	Ground
S1-AKN#	38	Acknowledge	A signal driven by an initiator to indicate an acknowledgment for a REQ/ACK data transfer handshake.
GND	39	Ground	Ground
S1-RST#	40	Reset	An "OR-tied" signal that indicates the RESET condition. The RST signal may be asserted by any SCSI device at any time.
GND	41	Ground	Ground
S1-MSG#	42	Message	A signal driven by a target during the MESSAGE phase.
GND	43	Ground	Ground
S1-SEL#	44	Select	An "OR-tied" signal used by an initiator to select a target or by a target to reselect an initiator. NOTE: The SEL signal was not defined as "OR-tied" in SCSI-1. It has been defined as "OR-tied" in SCSI-2. This does not cause an operational problem in mixing SCSI-1 and SCSI-2 devices.
GND	45	Ground	Ground

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PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
S1-C/D#	46	Control/Data	A signal driven by a target that indicates whether CONTROL or DATA information is on the DATA BUS. True indicates CONTROL.
GND	47	Ground	Ground
S1-REQ#	48	Request	A signal driven by a target to indicate a request for a REQ/ACK data transfer handshake.
GND	49	Ground	Ground
S1-I/O#	50	Input/Output	A signal driven by a target that controls the direction of data movement on the DATA BUS with respect to an initiator. True indicates input to the initiator. This signal is also used to distinguish between SELECTION and RESELECTION phases.

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5.16 J021 – IDE/ATA ATAPI-4 (44 Pin 2mm) Header

J021 is a 44-pin 2X22 (2MM pitch) header.

Table 18 Pinout – J021 – IDE/ATA Interface – 44 pin 2mm pitch

PIN NAME	PIN #	SIGNAL NAME	SIGNAL DESCRIPTION
PWRGOOD	1	Power Good	This signal is the Power Good output signal. It pulses low for 200 ms (typical, minimum 130 ms) when triggered by RSTSW# or by a Watchdog Timer Expired event, and it remains low whenever VCC is below the reset threshold or when the RSTSW# signal input is a logic low. This output signal remains low for 200ms (typical, minimum 130 ms) after one of the following occurs: VCC rises above the reset threshold, the watchdog triggers a reset, or the RSTSW# input signal goes low to high.
GND	2	Ground	Ground
A1-DD7	3	Data Bus 7	This signal is Data Bit 7 of the Data Bus that is connected to IDE Channel.
A1-DD8	4	Data Bus 8	This signal is Data Bit 8 of the Data Bus that is connected to IDE Channel.
A1-DD6	5	Data Bus 6	This signal is Data Bit 6 of the Data Bus that is connected to IDE Channel.
A1-DD9	6	Data Bus 9	This signal is Data Bit 9 of the Data Bus that is connected to IDE Channel.
A1-DD5	7	Data Bus 5	This signal is Data Bit 5 of the Data Bus that is connected to IDE Channel.
A1-DD10	8	Data Bus 10	This signal is Data Bit 10 of the Data Bus that is connected to IDE Channel.
A1-DD4	9	Data Bus 4	This signal is Data Bit 4 of the Data Bus that is connected to IDE Channel.
A1-DD11	10	Data Bus 11	This signal is Data Bit 11 of the Data Bus that is connected to IDE Channel.
A1-DD3	11	Data Bus 3	This signal is Data Bit 3 of the Data Bus that is connected to IDE Channel.
A1-DD12	12	Data Bus 12	This signal is Data Bit 12 of the Data Bus that is connected to IDE Channel.
A1-DD2	13	Data Bus 2	This signal is Data Bit 2 of the Data Bus that is connected to IDE Channel.
A1-DD13	14	Data Bus 13	This signal is Data Bit 13 of the Data Bus that is connected to IDE Channel.
A1-DD1	15	Data Bus 1	This signal is Data Bit 1 of the Data Bus that is connected to IDE Channel.
A1-DD14	16	Data Bus 14	This signal is Data Bit 14 of the Data Bus that is connected to IDE Channel.
A1-DD0	17	Data Bus 0	This signal is Data Bit 0 of the Data Bus that is connected to IDE Channel.

PIN NAME	PIN #	SIGNAL NAME	SIGNAL DESCRIPTION
A1-DD15	18	Data Bus 15	This signal is Data Bit 15 of the Data Bus that is connected to IDE Channel.
GND	19	Ground	Ground
N/C	20	N/C	Not connected
A1-DMARQ	21	DMA Request for IDE Master	This is the input pin from the IDE Channel DMA request to do the IDE Master Transfer. Use of this signal depends upon the type of board.
GND	22	Ground	Ground
A1-DIOW#	23	IO Write Command	This signal is the IOW command output pin to notify the IDE device that the available Write Data is already asserted by the onboard IDE controller.
GND	24	Ground	Ground
A1-DIOR#	25	IO Read Command	This signal is the IOR command output pin to notify the IDE device to assert the Read Data.
GND	26	Ground	Ground
A1-IORDY	27	IDE Ready	This is the input pin from the IDE Channel to indicate the IDE device is ready to terminate the IDE command. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready.
CSEL	28	Cable Select	Cable Select allows each device to determine whether it should configure itself as device 0 or device 1. On IDE buses which require this selection to be done using the cable select method, then this pin should be at GROUND potential. In this case, (a) if a single connector is being used on the QTB/Dxp board, then this connector (J021 or J022) should have it's corresponding grounding resistor installed at manufacturing time; or (b) if both on-board IDE connectors are being used, then the connector to be attached to device 0 (master device) should have its corresponding grounding resistor installed at manufacturing time, and the connector to be attached to device 1 (slave device) should not have its grounding resistor installed at manufacturing time. If the Cable Select method is not to be used (for example, drives self-configure using inter-drive communication), then this pin is typically a NO CONNECT. Please specify the Cable Select option (eg. the CSEL44 option is used for this 44-pin connector) at order time.
A1-DMACK#	29	DACK for IDE Master	This is the output pin to grant the IDE Channel DMA request to begin the IDE Master Transfer. Use of this signal depends upon the type of board.
GND	30	Ground	Ground
A1-INTRQ	31	IDE Interrupt	This is the input pin from the IDE Channel to signal an interrupt. It will be routed to the appropriate Int 14 8259 interrupt controller input. Depending upon the board type, this input may be steerable to other interrupt levels.

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PIN NAME	PIN #	SIGNAL NAME	SIGNAL DESCRIPTION
A1-IOCS16#	32	Device 16-Bit I-O	This is the input pin from the IDE device which, during PIO transfer modes 0, 1 or 2, indicates to the host system that the 16-bit data port has been addressed and that the device is prepared to send or receive a 16-bit data word.
A1-DA1	33	Address Bus 1	This signal is Address Bit 1 of the ATA Address Bus that is connected to IDE Channel.
QT_PDIAG-	34	Passed Diagnostics	This signal is asserted by Device 1 to indicate to Device 0 that it has completed diagnostics. Tie to Pin 34 of additional drive connectors for multiple drive configurations; This pin is NOT tied to the host IDE controller, rather it is used only for inter-drive communication.
A1-DA0	35	Address Bus 0	This signal is Address Bit 0 of the ATA Address Bus that is connected to IDE Channel.
A1-DA2	36	Address Bus 2	This signal is Address Bit 2 of the ATA Address Bus that is connected to IDE Channel.
A1-CS0#	37	Chip Select 1 for Ch 0	This is the Chip Select 1 command output pin to enable the IDE device to watch the Read/Write Command.
A1-CS1#	38	Chip Select 3 for Ch 1	This is the Chip Select 3 command output pin to enable the IDE device to watch the Read/Write Command.
QT_DASP-	39	Device Active, or Slave (Device 1) Present	This is a time-multiplexed signal that indicates that a device is active, or that Device 1 is present. Pin 39 of each of the two ATA/IDE headers on this board are tied together. Tie to Pin 39 of additional drive connectors for multiple drive configurations. This pin is NOT tied to the host IDE controller, rather it is used only for inter-drive communication.
GND	40	Ground	Ground
+5V	41	+5V	POWER +5V
+5V	42	+5V	POWER +5V
GND	43	Ground	Ground
N/C	44	N/C	Not connected

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5.17 J022 – IDE/ATA (40 Pin 0.100") Header

J022 is a 40-pin 2X20 (0.100" pitch) header.

Table 19 Pinout – J022 – IDE/ATA Interface – 40 pin 0.100" pitch

PIN NAME	PIN #	SIGNAL NAME	SIGNAL DESCRIPTION
PWRGOOD	1	Power Good	This signal is the Power Good output signal. It pulses low for 200 ms (typical, minimum 130 ms) when triggered by RSTSW# or by a Watchdog Timer Expired event, and it remains low whenever VCC is below the reset threshold or when the RSTSW# signal input is a logic low. This output signal remains low for 200ms (typical, minimum 130 ms) after one of the following occurs: VCC rises above the reset threshold, the watchdog triggers a reset, or the RSTSW# input signal goes low to high.
GND	2	Ground	Ground
A1-DD7	3	Data Bus 7	This signal is Data Bit 7 of the Data Bus that is connected to IDE Channel.
A1-DD8	4	Data Bus 8	This signal is Data Bit 8 of the Data Bus that is connected to IDE Channel.
A1-DD6	5	Data Bus 6	This signal is Data Bit 6 of the Data Bus that is connected to IDE Channel.
A1-DD9	6	Data Bus 9	This signal is Data Bit 9 of the Data Bus that is connected to IDE Channel.
A1-DD5	7	Data Bus 5	This signal is Data Bit 5 of the Data Bus that is connected to IDE Channel.
A1-DD10	8	Data Bus 10	This signal is Data Bit 10 of the Data Bus that is connected to IDE Channel.
A1-DD4	9	Data Bus 4	This signal is Data Bit 4 of the Data Bus that is connected to IDE Channel.
A1-DD11	10	Data Bus 11	This signal is Data Bit 11 of the Data Bus that is connected to IDE Channel.
A1-DD3	11	Data Bus 3	This signal is Data Bit 3 of the Data Bus that is connected to IDE Channel.
A1-DD12	12	Data Bus 12	This signal is Data Bit 12 of the Data Bus that is connected to IDE Channel.
A1-DD2	13	Data Bus 2	This signal is Data Bit 2 of the Data Bus that is connected to IDE Channel.
A1-DD13	14	Data Bus 13	This signal is Data Bit 13 of the Data Bus that is connected to IDE Channel.
A1-DD1	15	Data Bus 1	This signal is Data Bit 1 of the Data Bus that is connected to IDE Channel.
A1-DD14	16	Data Bus 14	This signal is Data Bit 14 of the Data Bus that is connected to IDE Channel.
A1-DD0	17	Data Bus 0	This signal is Data Bit 0 of the Data Bus that is connected to IDE Channel.

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PIN NAME	PIN #	SIGNAL NAME	SIGNAL DESCRIPTION
A1-DD15	18	Data Bus 15	This signal is Data Bit 15 of the Data Bus that is connected to IDE Channel.
GND	19	Ground	Ground
N/C	20	N/C	Not connected
A1-DMARQ	21	DMA Request for IDE Master	This is the input pin from the IDE Channel DMA request to do the IDE Master Transfer. Use of this signal depends upon the type of board.
GND	22	Ground	Ground
A1-DIOW#	23	IO Write Command	This signal is the IOW command output pin to notify the IDE device that the available Write Data is already asserted by the onboard IDE controller.
GND	24	Ground	Ground
A1-DIOR#	25	IO Read Command	This signal is the IOR command output pin to notify the IDE device to assert the Read Data.
GND	26	Ground	Ground
A1-IORDY	27	IDE Ready	This is the input pin from the IDE Channel to indicate the IDE device is ready to terminate the IDE command. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready.
CSEL	28	Cable Select	Cable Select allows each device to determine whether it should configure itself as device 0 or device 1. On IDE buses which require this selection to be done using the cable select method, then this pin should be at GROUND potential. In this case, (a) if a single connector is being used on the QTB/Dxp board, then this connector (J021 or J022) should have it's corresponding grounding resistor installed at manufacturing time; or (b) if both on-board IDE connectors are being used, then the connector to be attached to device 0 (master device) should have its corresponding grounding resistor installed at manufacturing time, and the connector to be attached to device 1 (slave device) should not have its grounding resistor installed at manufacturing time. If the Cable Select method is not to be used (for example, drives self-configure using inter-drive communication), then this pin is typically a NO CONNECT. Please specify the Cable Select option (eg. the CSEL40 option is used for this 40-pin connector) at order time.
A1-DMACK#	29	DACK for IDE Master	This is the output pin to grant the IDE Channel DMA request to begin the IDE Master Transfer. Use of this signal depends upon the type of board.
GND	30	Ground	Ground
A1-INTRQ	31	IDE Interrupt	This is the input pin from the IDE Channel to signal an interrupt. It will be routed to the appropriate Int 14 8259 interrupt controller input. Depending upon the board type, this input may be steerable to other interrupt levels.

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PIN NAME	PIN #	SIGNAL NAME	SIGNAL DESCRIPTION
A1-IOCS16#	32	Device 16-Bit I-O	This is the input pin from the IDE device which, during PIO transfer modes 0, 1 or 2, indicates to the host system that the 16-bit data port has been addressed and that the device is prepared to send or receive a 16-bit data word.
A1-DA1	33	Address Bus 1	This signal is Address Bit 1 of the ATA Address Bus that is connected to IDE Channel.
QT_PDIAG-	34	Passed Diagnostics	This signal is asserted by Device 1 to indicate to Device 0 that it has completed diagnostics. Tie to Pin 34 of additional drive connectors for multiple drive configurations; This pin is NOT tied to the host IDE controller, rather it is used only for inter-drive communication.
A1-DA0	35	Address Bus 0	This signal is Address Bit 0 of the ATA Address Bus that is connected to IDE Channel.
A1-DA2	36	Address Bus 2	This signal is Address Bit 2 of the ATA Address Bus that is connected to IDE Channel.
A1-CS0#	37	Chip Select 1 for Ch 0	This is the Chip Select 1 command output pin to enable the IDE device to watch the Read/Write Command.
A1-CS1#	38	Chip Select 3 for Ch 1	This is the Chip Select 3 command output pin to enable the IDE device to watch the Read/Write Command.
QT_DASP-	39	Device Active, or Slave (Device 1) Present	This is a time-multiplexed signal that indicates that a device is active, or that Device 1 is present. Pin 39 of each of the two ATA/IDE headers on this board are tied together. Tie to Pin 39 of additional drive connectors for multiple drive configurations. This pin is NOT tied to the host IDE controller, rather it is used only for inter-drive communication.
GND	40	Ground	Ground

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5.18 J023 – Floppy Disk Header

J023 is a 34-pin 2X17 (0.100" pitch) header.

Table 20 Pinout – J023 – Floppy Disk Interface 34 pin

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
GND	1	Ground	Ground
F1-DENSL0#	2	Density Select	This signal Indicates whether a low (250/300 Kb/s) or high (500/1000 Kb/s) data rate has been selected.
GND	3	Ground	Ground
N/C	4	N/C	Not connected
GND	5	Ground	Ground
GND	6	Ground	Ground
GND	7	Ground	Ground
F1-INDEX#	8	Index Status	This active low Schmitt Trigger input signal senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
GND	9	Ground	Ground
F1-MTR0#	10	Motor On 0	Active-low output selects motor drive 0.
GND	11	Ground	Ground
F1-DS1#	12	Drive Select 1	Active low, output selects drive 1.
GND	13	Ground	Ground
F1-DS0#	14	Drive Select 0	Active low, output selects drive 0.
GND	15	Ground	Ground
F1-MTR1#	16	Motor On 1	Active-low output selects motor drive 1.
GND	17	Ground	Ground
F1-DIR#	18	Direction	This active low output determines the direction of the head movement (low = step-in, high = step-out). During the write or read modes, this output is high.
GND	19	Ground	Ground
F1-STEP#	20	Step Head	This active low output signal produces a pulse at a software-programmable rate to move the head during a seek operation.
GND	21	Ground	Ground
F1-WDATA#	22	Write Serial Data	This active low output is a write- precompensated serial data to be written onto the selected disk drive. Each falling edge causes a flux change on the media.
GND	23	Ground	Ground
F1-WGATE#	24	Write Gate	This active-low, high-drive output enables the write circuitry of the selected disk drive. This signal prevents glitches during power-up and power-down. This prevents writing to the disk when power is cycled.
GND	25	Ground	Ground

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PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
F1-TRK0#	26	Track 00	This active low Schmitt Trigger input signal senses from the disk drive that the head is positioned over the outermost track.
GND	27	Ground	Ground
F1-WP#	28	Write Protected Status	This active-low Schmitt Trigger input signal senses from the disk drive that a disk is write-protected. Any write command is ignored.
GND	29	Ground	Ground
F1-RDATA#	30	Read Serial Data	This active-low, raw data read signal from the disk is connected here. Each falling edge represents a flux transition of the encoded data.
GND	31	Ground	Ground
F1-HDSEL#	32	Head Select	This active low output determines which disk drive head is active. Low = Head 0, high (open) = Head 1.
GND	33	Ground	Ground
F1-DKCHG#	34	Disk Change	This disk interface input indicates when the disk drive door has been opened. This active-low signal is read from bit D7 of address xx7h.

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5.19 J024 – USB Dual-Port Header

J024 is a 10-pin 2X5 (0.100" pitch) header. Either J024, J026 (section 5.21) or both can be populated.

Table 21 Pinout – J024 – USB Header – 10 pin

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
+5V	1	+5V	POWER +5V
+5V	2	+5V	POWER +5V
U1_D-	3	Channel 1 Data -	USB data channel 1 - negative signal
U2_D-	4	Channel 2 Data -	USB data channel 2 - negative signal
U1_D+	5	Channel 1 Data +	USB data channel 1 - positive signal
U2_D+	6	Channel 2 Data +	USB data channel 2 - positive signal
GND	7	Ground	Ground
GND	8	Ground	Ground
GND	9	Ground	Ground
GND	10	Ground	Ground

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5.20 J025 – Reset (4 Pin Right-Angle Momentary) Switch

This 4-pad connector is provided to accommodate a right-angle 4-pin 200 mil reset switch.

J025 is a SPST momentary-contact N.O. (normally open) type of switch. The button is parallel to the plane of the PCB and protrudes from the edge of the card.

Either J010 (section 5.6) or J025 may be populated (but not both at the same time).

Table 22 Pinout – J025 – Reset Interface – 4 Pin Right Angle SPST Momentary Switch

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
MR-RSTSW#	1	Manual Reset	Hard Reset Input, Active low. This signal drives the Manual-Reset Input. A logic low on this signal asserts system reset. Reset remains asserted as long as this signal is held low and for 200ms (typical; minimum 130ms) after this signal returns high. The active-low input has an internal 52kΩ pull-up resistor. It can be driven from a CMOS-logic line or shorted to ground with a switch. Leave open or connect to VCC (+5V) if unused.
GND	2	Ground	Ground
GND	3	Ground	Ground
GND	4	Ground	Ground

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5.21 J026 – USB (Dual Channel Stacking or Single Channel) Connector

J026 is a standard dual type-A (host) stacking connector for standard USB type-A plugs.

Note- this connector provides a Type-A connection to the Universal Serial Bus for each of two ports.

Table 23 Pinout – J026 – USB Connector – 8 pin

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
+5V	1	+5V	POWER +5V
U1_D-	2	Channel 1 Data -	Not Implemented – Future use
U1_D+	3	Channel 1 Data +	Not Implemented – Future use
GND	4	Ground	Ground
+5V	5	+5V	POWER +5V
U2_D-	6	Channel 2 Data -	Not Implemented – Future use
U2_D+	7	Channel 2 Data +	Not Implemented – Future use
GND	8	Ground	Ground

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5.22 J027 – PC Speaker Output Header

J027 is a 2-pin 1X2 (0.100" pitch) header.

Table 24 Pinout – J027 – PC Speaker Output Interface

PIN NAME	PIN#	SIGNAL NAME	SIGNAL DESCRIPTION
MS-SPKROUT	1	Speaker Output	This signal is used to control the Speaker Output and should connect to the Speaker.
GND	2	Ground	Ground

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6 Order Information

The Qtb/Dxp board can be ordered using the generic order model# given in this section. The general model# for the Qtb/Dxp is given below ("QTBDXP/" is the board identifier, which is followed by order option codes; each position in the order option code area of the model# that contains a dash character ('-') requires the dash character. There are 15 option positions which can be specified.

Model number format: **QTBDXP/CEFI-KMPR-STUV-hit**
Example: QTBDXP/3313-1122-4233-131

POS	OPTION	VALUE	CONN	REF	NOTES
ALL	ANY	0– NONE C– CUSTOM	ANY		You can use 0 or C for ANY option position in the model #
C	CONNECTOR (MASS I/O)	1– 5X11 RA Receptacle AMP 2– 5X22 RA Receptacle AMP 3– BOTH	J901 J902	5.1	This applies to the MASS I/O connector, which attached to the CPU board's mating connectors
E	ETHERNET	1– TELCO-8 10BASE-T 2– 2X8 (.100" PITCH) AUI HEADER 3– BOTH	J017 J016	5.13 5.12	
F	FLOPPY	1– 2X17 (.100" PITCH)	J023	5.18	
I	IDE	1– 2X20 (.100" PITCH) 40-PIN 2– 2X22 (2MM PITCH) 44-PIN 3– BOTH	J022 J021	5.17 5.16	See also option position "i" below
K	KEYBOARD	1– MINI DIN-6 CIRCULAR	J011	5.7	
M	MOUSE	1– MINI DIN-6 CIRCULAR	J012	5.8	
P	PRINTER	1– 2X13 (.100" PITCH) 2– (1) WITH EMI FILTER		5.4	EMI Filtering schematic will be supplied on request
R	RESET	1– SPST MOMENTARY N.O. VERT 2– SPST MOMENTARY N.O. R/A	J010 J025	5.6 5.20	
S	SERIAL	1– 1x 2X5 (.100" PITCH) COM1 2– 2x 2X5 (.100" PITCH) COM1/2 3– 3x 2X5 (.100" PITCH) COM1/2/3 4– 4x 2X5 (.100" PITCH) COM1/2/3/4	J004 J004-5 J004-6 J004-7	5.3	
T	SCSI	1– 2X25 (.100" PITCH) 50-PIN 2– (1) WITH ACTIVE TERMINATOR	J020	5.15	Active Terminator includes off/on jumper to enable/disable terminator
U	USB	1– DUAL PORT STACKING TYPE-A 2– 2X5 (.100" PITCH) HEADER 2-PORT 3– BOTH	J026	5.21	Dual stacking connector is a downstream (Type A) for the host
V	VIDEO	1– DSUB 15-PIN R/A (VGA) 2– 2X18 (.100" PITCH) PANEL HDR 3– BOTH	J014 J009	5.10 5.5	Standard PC VGA connector
h	MISC.	1– 2X3 (.100" PITCH) HEADER	J013	5.9	Miscellaneous power & other
i	IDE CSEL	1– CSEL40: CSEL ON 40-PIN GNDED 2– CSEL44: CSEL ON 44-PIN GNDED 3– BOTH			Two shunts apply each to the respective 40-pin or 44-pin IDE headers. See option position "I" above
t	SPEAKER	1– 1X2 (.100" PITCH) SPEAKER HDR	J027	5.22	

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7 Service Information

If you feel your board requires service, Megatel Service Department will do all it can to get you up and running – quickly.

If you purchased your board from a Distributor:
Our distributors are technically capable and will help you to determine and correct your problem. Since your proof of purchase was obtained from the Distributor, please return your board to them. Please follow their instructions for returning your board for service.

If you purchased your board directly from Megatel:
Please Call or Fax to Megatel's Service Department prior to shipping, to receive your RMA# (Return Materials Authorization number). You may also submit a request for an RMA# from our web site http://www.metatel.ca. Boards that do not have RMA#s will not receive priority. To receive an RMA#, you will be required to provide the following information:

1. Company Name
2. Board Model Number or Product Order Number
3. Board Serial Number
4. Description of the Problem
5. Purchase Order Number

Special Shipping Instructions
Along with the information on the Megatel SERVICE FORM (see next page), please include the following on one of your commercial invoices:

1. The value of the board(s) – this value must match the invoice(s) we sent with the boards
2. A copy of the invoice(s) we sent with the boards (Proof of Purchase)
3. Be sure to state one of the following
    a) "Canadian Goods Being Returned for Repair"
    b) "Canadian Goods Being Returned for Warranty Repair"
    c) "Canadian Goods Being Returned"

One copy of the above documents is to be placed inside the shipping box and one copy is to be placed on the outside of the shipping box (marked for CUSTOMS). Other products (i.e. disk drives, LCD panels, etc.) that were not purchased from Megatel, but will be used as part of the servicing of the returned board, must be shipped separately and listed in the Megatel SERVICE FORM (next page) under "Equipment Sent Separately" heading. Products not purchased from Megatel should be shipped under a temporary import license of the maximum time limit.

Send PREPAID to the SERVICE DEPT. at:

MEGATEL COMPUTER CORPORATION
125 WENDELL AVENUE
WESTON, ONTARIO
M9N 3K9 CANADA

Our harmonized Number: 8471.92.00

Call us at +1 416 245-2953 between the hours of 9.00 am to 5.00 pm EST. Or you may send megatel a Fax using the phone number +1 416 245-6505.

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Megatel SERVICE FORM

PRIOR TO SHIPPING:: Please call Megatel to receive your RMA#. Only boards sent with an RMA# will be given priority. This RMA# must appear on all paper work and be clearly marked on the outside of the shipping box.

RMA#: ______________________

Date Called: ______________________

Your Company Name: ______________________

Your Contact Name: ______________________

Your Company Address:

Ship To: ______________________ **Bill To:** ______________________

______________________ ______________________

______________________ ______________________

______________________ ______________________

Your Telephone Number: ______________________ **Extension:** __________

Your Fax Number: ______________________ **Extension:** __________

Equipment You are Sending to Us: Pleasefill in the following as completely and accurately as possible

Product #	Serial #	Description of the Problem

Purchase Order Number for this Return ______________________

Equipment Sent Separately

Courier	Waybill#	Description (include Model#, Serial#)

Courier Company to be Used for Returning this Shipment: Please Circle or Check One

FEDEX	EMERY	UPS AIR	PUROLATOR	ALPHA	TRANS	BAISLEY

OTHER __________

Special Instructions/Comments You have for us: ______________________

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8 Qtb/Dxp Physical Board Specifications

This diagram applies to Qtb/Dxp v3.00 PCB.